Abstract
This document describes the hardware features and specifications of the cost effective AMY-6M GPS module featuring the u-blox 6 positioning engine.

The AMY-6M module boasts the industry’s smallest form factor and is a fully tested standalone solution that requires no host integration. This module combines exceptional GPS performance with highly flexible power, design, and serial communication options.
## Document Information

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### This document applies to the following products:

<table>
<thead>
<tr>
<th>Name</th>
<th>Type number</th>
<th>ROM/FLASH version</th>
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<td>AMY-6M</td>
<td>AMY-6M-0-000</td>
<td>ROM6.02</td>
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<td>AMY-6M</td>
<td>AMY-6M-0-001</td>
<td>ROM7.03</td>
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Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

- **GPS Compendium:** This document, also known as the GPS book, provides a wealth of information regarding generic questions about GPS system functionalities and technology.
- **Receiver Description including Protocol Specification:** Messages, configuration and functionalities of the u-blox 6 software releases and receivers are explained in this document.
- **Application Note:** document provides general design instructions and information that applies to all u-blox GPS receivers. See Section Related documents for a list of Application Notes related to your GPS receiver.

How to use this Manual

The AMY-6M Hardware Integration Manual provides the necessary information to successfully design in and configure these u-blox 6-based GPS receiver modules. For navigating this document please note the following:

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:

- **An index finger points out key information pertaining to module integration and performance.**
- **A warning symbol indicates actions that could negatively impact or damage the module.**

Questions

If you have any questions about u-blox 6 Hardware Integration, please:

- Read this manual carefully.
- Read the questions and answers on our FAQ database on the homepage [http://www.u-blox.com](http://www.u-blox.com)
- Contact our information service on the homepage [http://www.u-blox.com](http://www.u-blox.com)

Technical Support

Worldwide Web

Our website (www.u-blox.com) is a rich pool of information. Product information, technical documents and helpful FAQ can be accessed 24h a day.

By E-mail

If you have technical problems or cannot find the required information in the provided documents, contact the nearest of the Technical Support offices by email. Use our service pool email addresses rather than any personal email address of our staff. This makes sure that your request is processed as soon as possible. You will find the contact details at the end of the document.

**Helpful Information when Contacting Technical Support**

When contacting Technical Support please have the following information ready:

- Receiver type (AMY-6M) and firmware version (e.g. V6.02)
- Receiver configuration
- Clear description of your question or the problem together with a u-center logfile
- A short description of the application
- Your complete contact details
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1 Hardware description

1.1 Overview

The AMY-6M is the GPS industry’s smallest standalone receiver. It is a fully tested ROM-based solution that features the high performance u-blox 6 positioning engine. The AMY-6M has been developed for easy design and integration and requires no host integration, which enables extremely short times to market.

The AMY-6M offers four different serial interfaces. The receiver provides fast acquisition and excellent tracking performance at an economical price. Furthermore, 2-layer PCB integration is supported, which brings additional cost savings.

AMY-6M’s miniature size means that it can be integrated into the smallest portable devices. Advanced interference suppression mechanisms and innovative RF architecture ensure maximum performance even in hostile signal environments.

1.2 Architecture

The AMY-6M module consists of two functional parts - the RF and the Baseband sections. See Figure 1 for a block diagram of the AMY-6M.

The RF section includes the DC-block, the RF input matching, the SAW bandpass filter, the u-blox 6 RF-IC (with integrated LNA) and the Crystal.

The Baseband section contains the u-blox 6 Baseband processor.

An RTC crystal and additional elements such as an external memory for enhanced programmability and flexibility are optional.

Figure 1: AMY-6M hardware block schematic
2 Design-in

In order to obtain good performance with a GPS receiver module, there are a number of points that require careful attention during the design-in. These include:

- **Power Supply**
  Good performance requires a clean and stable power supply.

- **Interfaces**
  Ensure correct wiring, rate and message setup on the module and your host system.

- **Antenna interface**
  For optimal performance seek short routing, matched impedance and no stubs.

> With AMY-6M an additional external LNA is mandatory if no active antenna is used.

2.1 Power management

2.1.1 Overview

The power supply circuitry can be adapted to various concepts, depending on the intended application. Figure 2 gives an overview of the power supply features.

![Power supply diagram](image)

**Figure 2: Power supply diagram**

2.1.1.1 Main supply voltage

During operation the base-band supply current is supplied through the V_DCDC pin. The built-in LDO generates the stabilized core voltage VDD_C from V_DCDC. The current at V_DCDC depends heavily on the current system state and is in general very dynamic.

> Use a low-impedance supply (<< 1 Ohm) at the V_DCDC pin.
u-blox 6 supports use of an external DC/DC converter for improved power efficiency supplying V\_DCDC and eventually the RF section. The DCDC\_EN signal allows shutting down this external DC/DC converter when V\_DCDC is not needed. If the DCDC\_EN signal shall be used, VDD\_IO must be supplied independently of the DC/DC converter, i.e. these voltages must be supplied even if the DC/DC converter is disabled.

2.1.1.2 Base-band I/O supply voltage
The digital I/Os of the base-band part are supplied with VDD\_IO from the host system. The wide range of VDD\_IO allows seamless interfacing to standard logic voltage levels.

\[ \text{VDD\_IO must be supplied in order for the system to boot.} \]

2.1.1.3 Base-band core voltages
The core voltages VDD\_B and VDD\_C core are generated separately to enable main supply VDD\_C switch off while the back-up domain VDD\_B remains alive. The core voltages are generated by means of internal LDOs. The input voltage range of the LDOs is wide and allows the use of several types of batteries.

2.1.1.4 Backup power supply
A backup battery can be connected to V\_BCKP to supply the RTC and backup RAM in case of power failure at the main battery for backup domain (VDD\_IO). An internal switch supplies the internal VDD\_B power domain in case VDD\_IO drops below the specified minimum value. VDD\_IO will supply the VDD\_B power domain if a sufficiently high input voltage is detected. See Figure 3 below and see also section 2.1.1.6.

\[ \text{Figure 3: Supply of Backup Domain (VDD\_B)} \]

\[ \text{Limit V\_BCKP and VDD\_IO to 3.6 V.} \]

2.1.1.5 RF supply voltages
The RF unit is supplied through the VDD\_RF pin. This supply voltage can optionally be generated internally with an LDO from the VDD\_3V input. If the supply voltage is 1.8 V, then the VDD\_3V must be shorted to the VDD\_RF pin, so that the internal LDO is shorted and there is no voltage drop.

Depending on the application, the RF supply voltage can be supplied from 3 different sources:
1. From the V\_DCDC node of the baseband power supply, taking advantage of the optional DC/DC converter.
2. From the VDD\_IO node, in cases where the Main Battery voltage and/or V\_DCDC are lower than the minimum RF supply voltage.
3. From a source independent of the baseband power management pins, e.g. the Main Battery node or a totally independent voltage source.

In all 3 cases, the connections to VDD\_3V and VDD\_RF must be made according to the supply voltage range that is actually supplied.

The RF supply voltage shall be free of noise and low frequency modulations.

There are two other LDOs in the RF unit providing improved supply rejection at very low dropout voltage for the noise sensitive parts of the RF-circuits.

\[ \text{Insert a ferrite bead (FB1) to isolate the RF supply from digital noise.} \]
2.1.1.6 Built-in supply voltage monitors

Built-in supply voltage monitors ensure that the system always operates within safe limits. The following conditions need to be met in order for the system to run properly:

1. The core voltages VDD_C and VDD_B need to be within specification. These voltages are supervised by internal supply monitors.
2. The I/O voltage VDD_IO needs to be within specification. This voltage is supervised by an internal supply monitor. This supply monitor has a system configurable threshold done automatically by the Firmware.
3. The RF supply voltage needs to be within specification. This voltage is supervised at pin V_RESET by an internal supply monitor. The threshold of this supply monitor can be configured using the V_TH pin. If V_TH is open, the threshold is set for a nominal supply voltage of 1.8 V, if this pin is connected to GND the threshold is set for a nominal supply voltage of 2.5 V and above.
4. If external memory is used, its supply voltage, i.e. VDD_IO, needs to be within the specification of this part.

With respect to points 2 and 3 listed above, the voltage that defines the lowest operational boundary condition of the system shall be supervised at the V_RESET pin. This is usually the RF IC supply voltage (VDD_3V). In designs using EEPROM memory it may also be VDD_IO. Normally, higher system supply voltages take longer to rise and fall faster than lower supply voltages, e.g. if in a given application, the RF section requires 1.8 V but external memory requires 2.7 V, it is advisable to monitor VDD_IO rather than VDD_3V.

With respect to item 4 above the design must ensure that VDD_IO is present and within the operating range of the external memory at system boot time. Else, the system may fail in detecting the external memory and the memory will be ignored.

Initially at system start-up, the threshold of the VDD_IO supply monitor is set to its lowest value in order to ensure the system only starts when I/Os are operational. Once external memory is detected, the threshold will be adapted according to memory type in order to detect brown-out conditions in case VDD_IO would drop below the operational range of external memory. The following rules do apply:

1. In case of EEPROM at DDC interface, the VDD_IO threshold is set to 1.8V. All EEPROMs used with u-blox 6 must support operation down to 1.8V. Only EEPROM types listed in Table 14 must be used.
2. In case of Serial FLASH memory at SPI interface, VDD_IO threshold is set according to its type. Only FLASH memory types listed in Table 15 must be used.

Internally, VDD_B and VDD_C are supervised by power-on reset circuits. Reset signals on backup and core domains are only released once the respective supply voltages fall within the operational conditions.

After release of the power-on reset on circuit at VDD_C the systems waits for 2048 clock cycles to stabilize before the clock signal is fed into the core. This ensures system operation only with a clean clock signal.

An additional monitor switches the supply of the back-up region VDD_B (RTC and backup RAM) from VDD_IO to V_BCKP, once VDD_IO falls below its operational specification. Thus, a separate supply source can be used to maintain RTC and backup RAM information even if VDD_IO fails. If this feature is not needed, V_BCKP must be connected to GND.

2.1.1.7 USB interface power supply

VDD_USB supplies the I/Os of the USB interface. If the USB interface is not used, the VDD_USB pin must be connected to GND.

If the USB interface is being used the system can be either self-powered, i.e. powered independently from the USB bus, or it can be bus-powered, i.e. powered through the USB connection. In bus-powered mode, the system supply voltages need to be generated from the USB supply voltage VBUS. See section 2.3.2.

If the application uses USB, the correct USB power mode needs to be configured (bus-powered or self powered). See the u-blox 6 Receiver Description including Protocol Specification [1].
2.1.2 Power management configuration

Depending on the application, the power supply schematic will differ. Some examples are shown in the following sections:

- Supply voltage nominal 3.3 V (2.5–3.6V)  
  see section 2.1.5
- Supply voltage nominal 1.8 V (1.75–2.0V)  
  see section 2.1.6
- Direct supply of core voltages (1.75–2.0V for RF part, 1.4–3.6V for digital part)  
  see section 2.1.7
- Dual power supply using 3.0V and 1.4V (VDD_3V 3.0 V, V_DCDC 1.4 V)  
  see section 2.1.8
- Use of external DCDC converter 1.8V (1.75–2.0V)  
  see section 2.1.9

2.1.3 System power consumption

This chapter is targeted at the design and dimensioning of the system power supply. In order to analyze the power consumption and supply currents for various scenarios, Table 1 lists the respective supply currents at the minimum supply voltages which are 1.4V for the baseband part and 1.8V for the RF part. Table 1 further shows the power consumption if the RF section needs to be supplied with 2.5V

<table>
<thead>
<tr>
<th>Continuous mA</th>
<th>Acquisition mA</th>
<th>BB 1.4 V / RF 1.8 V Continuous mW</th>
<th>Acquisition mW</th>
<th>BB 1.4 V / RF 2.5 V Continuous mW</th>
<th>Acquisition mW</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF-IC 20</td>
<td>20</td>
<td>36</td>
<td>36</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>BB-IC 17</td>
<td>27</td>
<td>24</td>
<td>38</td>
<td>24</td>
<td>38</td>
</tr>
<tr>
<td>Total 37</td>
<td>47</td>
<td>60</td>
<td>74</td>
<td>74</td>
<td>88</td>
</tr>
</tbody>
</table>

Table 1: Raw Current and Power Consumption (ECO Mode, moderate signal levels)

Table 2 and Table 3 compare the approximate power consumption for the different scenarios and different system supply voltages. Table 2 shows the continuous power consumption when the system has acquired all satellites and is running in steady state. Table 3 shows the peak power consumption during signal acquisition. These two cases allow assessing the dimensioning of peak power and continuous power capabilities of the power supply circuit. The green and red highlighting illustrates the best and the worst solution in terms of power consumption.

The following 2 scenarios are being compared:

1. Using linear regulators (LDO) only. For supply voltages up to 3.6 V the built-in LDOs of u-blox 6 can be used. For higher supply voltages, an additional external LDO is needed. There is no effect on power consumption or efficiency regardless whether external or built-in LDOs are being used.

2. Using an additional external single output voltage DC/DC converter to generate the intermediate system supply voltage of 1.8V which then is further regulated by the individual LDOs of base-band and RF-IC.

The maximum system supply voltage is only limited by the external DC/DC converter being used.

For the DC/DC converter, an efficiency of 80% has been assumed in calculating the power values shown in Table 2 and Table 3. If power-efficiency at high system supply voltages is key for the application, use of an ultra-high efficiency external DC/DC converter such as Linear Technology’s LTC3410 (2.0 × 2.0 mm² SC70 package) is recommended.

<table>
<thead>
<tr>
<th>Supply Voltage V</th>
<th>LDO [mW]</th>
<th>Single 1.8V DCDC Converter [mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8</td>
<td>67</td>
<td>83</td>
</tr>
<tr>
<td>2.5</td>
<td>93</td>
<td>83</td>
</tr>
<tr>
<td>3</td>
<td>111</td>
<td>83</td>
</tr>
<tr>
<td>3.3</td>
<td>122</td>
<td>83</td>
</tr>
<tr>
<td>4.2</td>
<td>155</td>
<td>83</td>
</tr>
<tr>
<td>5</td>
<td>185</td>
<td>83</td>
</tr>
</tbody>
</table>

Table 2: Continuous Tracking Power Consumption (ECO Mode)
### Table 3: Acquisition Power Consumption (ECO Mode)

<table>
<thead>
<tr>
<th>Supply Voltage [V]</th>
<th>LDO [mW]</th>
<th>Single 1.8V DCDC Converter [mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8</td>
<td>85</td>
<td>106</td>
</tr>
<tr>
<td>2.5</td>
<td>118</td>
<td>106</td>
</tr>
<tr>
<td>3</td>
<td>141</td>
<td>106</td>
</tr>
<tr>
<td>3.3</td>
<td>155</td>
<td>106</td>
</tr>
<tr>
<td>4.2</td>
<td>197</td>
<td>106</td>
</tr>
<tr>
<td>5</td>
<td>235</td>
<td>106</td>
</tr>
</tbody>
</table>

Some conclusions from Table 1 to Table 3:

- The most efficient solution is to have a direct 1.4 V / 1.8 V supply available from the system. The respective application circuit is shown in section 2.1.7.
- If a 1.8V supply is available the best solution is to supply RF and BB part directly. The respective application circuit is shown in section 2.1.6.
- For supply voltages above 2.5 V, a DC/DC converter having a 1.8 V output voltage should be used for good efficiency. The respective application circuit is shown in section 2.1.9.
- Using only the built-in LDOs of u-blox 6 at supply voltages between 2.5 V and 3.6 V is not efficient but very cost effective in terms of BoM. The respective application circuit is shown in section 2.1.5.

### 2.1.4 How to connect the power supply pins

Table 4 lists the power supply pins and their connection requirements.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DCDC</td>
<td>Main Core (VDD_C) Supply</td>
<td>Always needs input. The current consumption varies over time (peak currents). Keep series resistance low to prevent ripple on the power supply.</td>
</tr>
<tr>
<td>VDD_3V</td>
<td>Main RF Supply</td>
<td>Supplied by 2.5…3.6V or connected to VDD_RF, depends on supply scheme.</td>
</tr>
<tr>
<td>VDD_IO</td>
<td>I/O Supply Voltage</td>
<td>Always needs to be supplied.</td>
</tr>
<tr>
<td>V_BCKP</td>
<td>Backup voltage (VDD_B) supply</td>
<td>Connect to GND if not used.</td>
</tr>
<tr>
<td>VDD_B</td>
<td>Backup Core Voltage</td>
<td>Leave open.</td>
</tr>
<tr>
<td>VDD_C</td>
<td>Main Core Voltage</td>
<td>Leave open.</td>
</tr>
<tr>
<td>VDD_RF</td>
<td>RF Core Supply Voltage</td>
<td>Leave open or must be supplied by 1.75…2.0V, depends on supply scheme.</td>
</tr>
<tr>
<td>VDD_ANA</td>
<td>Analog Power</td>
<td>Leave open.</td>
</tr>
<tr>
<td>VDD_LNA</td>
<td>LNA Power Supply</td>
<td>Leave open.</td>
</tr>
<tr>
<td>V_RESET</td>
<td>RESET input</td>
<td>Connect to supervising voltage, mostly to VDD_3V (see 2.1.1.6)</td>
</tr>
<tr>
<td>V_TH</td>
<td>Sets Threshold for V_RESET</td>
<td>V_TH = open: V_RESET supervised voltage at nominal 1.8 V. V_TH= GND: V_RESET supervised voltage at nominal 2.5 V and above.</td>
</tr>
<tr>
<td>DCDC_EN</td>
<td>Enable for external DCDC converter</td>
<td>Leave open if not used. Otherwise connect to enable pin of external DCDC converter.</td>
</tr>
<tr>
<td>VDD_USB</td>
<td>Supply for USB interface</td>
<td>Connect to GND if not used.</td>
</tr>
</tbody>
</table>

Table 4: Power Supply Pins
2.1.5 Single 2.5…3.6 V supply

A single 3.0V power supply is very easy to design but is not the most efficient solution to run u-blox 6 receivers (see section 2.1.3 for details).

Figure 4: Single 2.5…3.6 V supply.

2.1.6 Single 1.75…2.0 V supply

The single 1.8V power supply is a very efficient configuration to run u-blox 6 receivers (see section 2.1.3 for details).

Figure 5: Single 1.75…2.0 V supply
2.1.7 Separate supplies of 1.8 V (1.75…2.0V) and 1.4 V (1.4…3.6V)

The dual 1.8V and 1.4V power supply the most efficient configuration to run u-blox 6 receivers (see section 2.1.3 for details). It assures stability since the sensitive RF supply is well separated from the fluctuating base band power supply.

![Figure 6: Separate supplies of 1.8 V and 1.4 V](image)

2.1.8 Separate supplies of 3.0 V (2.5…3.6 V) and 1.4 V (1.4…3.6 V)

It assures a better stability than a single 3.0V power supply as the sensitive RF supply is well separated from the fluctuating base band power supply.

![Figure 7: Dual supplies of 3.0 V and 1.4 V](image)
2.1.9 External 1.8V DCDC converter

The external DCDC converter providing 1.8V is the most efficient solution for main supply voltages above 2.5V.

![Diagram of AMY-6M](image)

Figure 8: External 1.8V DCDC converter

2.1.10 Operating modes

The u-blox AMY-6M features one continuous operating mode (Eco Mode).

**Eco Mode**

In Eco Mode, u-blox AMY-6M uses the acquisition engine to search for new satellites only when needed for navigation:

- In cold starts, u-blox AMY-6M searches for enough satellites to navigate and optimizes use of the acquisition engine to download their ephemeris.
- In non-cold starts, u-blox AMY-6M focuses on searching for visible satellites whose orbits are known from the Almanac.

In Eco Mode, the u-blox AMY-6M acquisition engine limits use of its searching resources to minimize power consumption.

u-blox AMY-6M deactivates the acquisition engine as soon as a position is fixed and a sufficient number (at least 4) of satellites are being tracked. The tracking engine continues to search and track new satellites without orbit information.

Power Save Mode and Maximum Performance Mode are not supported by AMY-6M.

**Power Save Mode requires an external RTC crystal to schedule system wake-up at pre-defined intervals.**
### 2.1.11 Active antenna supply

With AMY-6M active antennas are supplied via an external coil or circuit. AMY-6M does not provide the antenna bias voltage for active antennas on the RF_IN pin as other u-blox modules do. It is therefore necessary to provide this voltage outside the module via an inductor as indicated in Figure 9. u-blox recommends using an inductor from Murata (LQG15HS27NJ02). Alternative parts can be used if the inductor’s resonant frequency matches the GPS frequency of 1575.42MHz.

![Figure 9: Recommended wiring for active antennas](image)

For C and L values see Component Selection Section B.

- For optimal performance, it is important to place the inductor as close to the microstrip as possible. Figure 10 illustrates the recommended layout and how it should not be done.

![Figure 10: Recommended layout for connecting the antenna bias voltage for AMY-6M](image)
2.2 System functions

2.2.1 EXTINT - external interrupt pin
EXTINT0 and EXTINT1 are external interrupt pins. It can be used for wake-up functions in low-power modes. See the u-blox 6 Receiver Description including Protocol Specification [2].

2.2.2 System monitoring
The u-blox 6 GPS Receiver provides System Monitoring functions that allow the operation of the embedded processor and associated peripherals to be supervised. These System Monitoring functions are being output as part of the UBX protocol, class ‘MON’.
Please refer to the u-blox 6 Receiver Description including Protocol Specification [2]. For more information on UBX messages, serial interfaces for design analysis and individual system monitoring functions.

2.2.3 Interference Monitor
New with firmware version 7 and above is the Interference Monitor feature. In contrast to the CW Jamming Indicator, it is designed to detect both broad band and narrow band jammers. The receiver monitors the background noise and reports any abnormal behavior.

For more information about the Interference Monitor refer to the u-blox 6 Receiver Description including Protocol Specification [2].

2.3 Interfaces
u-blox AMY-6 receivers offer a number of different interfaces that can be used to connect to a host CPU: UART, USB, DDC (i2C compatible), and SPI. Depending on the application any of these interfaces may be selected.

For debugging purposes it is recommended to have a second interface (unused by the actual application) available on test-points.

New with firmware version 7 and above is the feature that each interface can define a corresponding pin, which indicates if bytes are ready to be transmitted. The Tx-ready pin can be selected from all PIOs which are not in use. Each Tx-ready pin is exclusively for one interface and cannot be shared.

See u-blox 6 Receiver Description including Protocol Specification [2] for description of the communication protocols available at these interfaces and the respective configuration options.

2.3.1 UART
UART 1 (RxD1/TxD1) is the default serial interface. It supports data rates from 4.8 kbit/s to 115.2 kbit/s. An interface based on RS232 standard levels (+/- 12 V) can be realized using external level shifters such as Maxim MAX3232.

For the default settings on the messages on UART1 see the AMY-6M Data Sheet [1]. Hardware handshake signals and synchronous operation are not supported.

2.3.2 USB
The u-blox 6 USB interface supports the full-speed data rate of 12 Mbit/s.

2.3.2.1 USB external components
The USB interface requires some external components in order to implement the physical characteristics required by the USB 2.0 specification. These external components are shown in Figure 11 and listed in Table 5.

In order to comply with USB specifications, VBUS must be connected through an LDO (U4) to pin VDD_USB of the module.
The AMY-6M can be either bus-powered or self-powered. Bus-powered means the AMY-6M is supplied by the VBUS voltage from the USB. Self-powered means the AMY-6M is powered by another supply independent from VBUS supply and just the USB interface VDD_USB is supplied by VBUS (through an LDO (U4)).

Depending on the characteristics of the LDO (U4) it is recommended to add a pull-down resistor (R11) at its output to ensure VDD_USB is not floating if LDO (U4) is disabled or the USB cable is not connected i.e. VBUS is not supplied.

All u-blox 6 receivers support both Bus and Self Powered Mode on the USB interface. Please be sure to use the latest drivers from our website.

- Connect VDD_USB to GND if not used.
- With config pin CFG_COM0 the AMY-6M can be set to Bus (CFG_COM1=open) or Self Powered (CFG_COM1=GND)
- USB is not compatible with Power Save Mode with FW6.02 and below

![Figure 11: USB Interface (bus powered setup)]

### Table 5: Summary of USB external components

<table>
<thead>
<tr>
<th>Name</th>
<th>Component</th>
<th>Function</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>U4</td>
<td>LDO</td>
<td>Regulates VBUS (4.4 ... 5.25 V) down to a voltage of 3.3 V.</td>
<td>Almost no current requirement (~1 mA) if the GPS receiver is operated as a USB self-powered device, but if bus-powered LDO (U4) must be able to deliver the maximum current of ~ 70 mA. A low-cost DC/DC converter such as LTC3410 from Linear Technology may be used as an alternative.</td>
</tr>
<tr>
<td>C23, C24</td>
<td>Capacitors</td>
<td>Required according to the specification of LDO U4</td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>Protection diodes</td>
<td>Protect circuit from overvoltage / ESD when connecting.</td>
<td>Use low capacitance ESD protection such as ST Microelectronics USBLC6-2.</td>
</tr>
<tr>
<td>R4, R5</td>
<td>Serial termination resistors</td>
<td>Establish a full-speed driver impedance of 28…44 Ohms</td>
<td>A value of 22 Ohms is recommended.</td>
</tr>
<tr>
<td>R11</td>
<td>Resistor</td>
<td>Ensures a pull down when LDO is disabled.</td>
<td>1k Ohms is recommended for USB self-powered setup. For bus-powered setup R11 is not required.</td>
</tr>
<tr>
<td>FB1</td>
<td>Ferrite Bead</td>
<td>Filters Noise at GPS frequency</td>
<td></td>
</tr>
</tbody>
</table>
2.3.3 Display Data Channel (DDC)

An I2C compatible Display Data Channel (DDC) interface is available for serial communication. For more information about DDC implementation refer to the u-blox 6 Receiver Description including Protocol Specification [2]. Background information about the DDC interface is available in Appendix C.1.

u-blox 6 GPS receivers normally run in I2C slave mode. Master Mode is only supported when external EEPROM is used to store configuration, at this time no other nodes may be connected to the bus. In this case, the receiver attempts to detect the EEPROM by writing and reading from a specific location.

Pins SDA2 and SCL2 have internal pull-ups. These pull-up resistors integrated in the pads of the baseband-IC are sufficient for most applications. However, for high capacitive loads, parallel external pull-up resistors need to be added. Table 6 lists the externally required pull-up resistor values for the DDC interface.

```
<table>
<thead>
<tr>
<th>Load Capacitance</th>
<th>Pull-Up Resistor Value R20, R21</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 pF</td>
<td>N/A</td>
</tr>
<tr>
<td>100 pF</td>
<td>18 kΩ</td>
</tr>
<tr>
<td>250 pF</td>
<td>4.7 kΩ</td>
</tr>
</tbody>
</table>
```

Table 6: Pull-up resistor values for DDC interface

2.3.3.1 Communicating to an I2C EEPROM with the GPS receiver as I2C master

Serial I2C memory can be connected to the DDC interface as shown in Figure 12. This can be used to permanently save configuration settings. It will automatically be recognized by firmware. The memory address must be set to 0b10100000 see Figure 12 (A0, A1 and A2 must be connected to GND), and the size must be to 4 kByte (32 kBit).

The AMY-6M monitors the supply voltage VDD_IO. This implies the I2C EEPROM is operating above the VDD_IO threshold defined for I2C EEPROM operation (see Section 2.1.1.6).

Only use I2C EEPROM types listed in Table 14

![Figure 12: Connecting external serial I2C memory used by the AMY-6M to save configuration (see EEPROM data sheet for exact pin orientation)](image)

In limited cases u-blox 6 GPS receivers can fail to correctly write to external I2C EEPROM. To guarantee successful storage of the configuration into external I2C EEPROM, the writing cycles need to be verified by a read cycle (see u-blox 6 firmware version 7 Release Notes [5] for details).

2.3.3.2 Communicating as I2C slave to a host

An I2C master can communicate with the AMY-6M through the DDC interface.
Figure 13: Connecting external serial I²C memory used by external host (see data sheet for exact pin orientation)

Note that the case shown on Figure 12 is different than the case when EEPROM is present but used by external host / CPU as indicated on Figure 13. This is allowed but precaution is required to ensure that the GPS receiver does not detect the EEPROM device, which would effectively configure the GPS receiver to be MASTER on the bus causing collision with the external host.

To ensure that the EEPROM device (connected to the bus and used by the host) is not detected by the GPS receiver it is important to set the EEPROM’s address to a value different than 0b1010000. This way EEPROM remains free to be used for other purposes and the GPS receiver will assume the SLAVE mode.

Ensure that at the start up the host allows enough time for the receiver to communicate over the bus to establish presence of the EEPROM. It is only when this interrogation is complete that the host can exercise full control over the bus (MASTER mode).

The AMY-6M always interrogates external EEPROM at the start-up. The interrogation process is guaranteed to complete within 250ms upon start up. This is the time the external host has to give to the ROM based GPS receiver to complete the EEPROM interrogation.

The AMY-6M DDC interface supports serial communication with u-blox wireless modules. See the specification of the applicable wireless module to confirm compatibility.

TX ready signal (data ready to be picked up) can be activated, for configuration see 2.4.1.3.

2.3.4 SPI

A Serial Peripheral Interface (SPI) is available. The SPI allows for the connection of external devices with a serial interface, e.g. FLASH memories or A/D converters, or to interface to a host CPU. Background information about the SPI interface is available in Appendix C.2.

2.3.4.1 Connecting SPI FLASH memory

SPI FLASH memory can be connected to the SPI interface to save AssistNow Offline data and/or receiver configuration. It will automatically be recognized by firmware when connected to SS_N.

Figure 14 shows how external memory can be connected. Note that an external voltage is required to power the FLASH (VDD_IO on the receiver is an input). Minimum SPI FLASH memory size is 1 Mbit.
Only use Serial FLASH types listed in Table 15.

It is not recommended to use Serial Flash at SPI for new designs.

The SPI signals at AMY-6M are at VDD_IO voltage levels. VDD_IO must be supplied with same voltage as external serial FLASH.

2.3.4.2 Detection of SPI serial FLASH

The AMY-6M only detects the serial FLASH if all the SPI pins (CLK, SS_N, MOSI and MISO) are high. This is the case if only the serial FLASH is connected to the SPI interface pins.

2.3.4.3 SPI communication (connecting to an SPI host/master)

Figure 16 shows how to connect an AMY-6M to a host/master. The signal on the pins must meet the conditions specified in the Data Sheet.
Figure 16: Connecting to SPI Host/Master

With AMY-6M the SPI MOSI, MISO and SCK pins share a configuration function at start up. Afterwards the SPI function will not affect the configuration pins. This might be difficult in case several slaves are connected to the host. In this case the problem can be solved as shown in Figure 17 by making sure the SS_N is high when the receiver starts up.

The SPI signals at AMY-6M are at with VDD_IO voltage levels. VDD_IO must be supplied with the same voltage as the host processor.

TX ready signal (data ready to be picked up) can be configured, see 2.4.1.3.

2.3.4.4 Pin configuration with module as one of several slaves

Figure 17: Diagram of SPI Pin Configuration

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
<th>Model</th>
<th>Supplier</th>
</tr>
</thead>
<tbody>
<tr>
<td>U_i – U_j</td>
<td>Buffer</td>
<td>NC7SZ125</td>
<td>Fairchild</td>
</tr>
</tbody>
</table>

Figure 18: Recommended components for SPI pin configuration

Use same power voltage to supply U_i – U_j and VDD_IO.
2.4 I/O Pins

2.4.1 Peripheral Input Output (PIO)

All PIOs have internal pull-ups or pull-downs (PIO9 only). Thus there is no need to connect PIOs to GND or VDD if not used.

A signal change on pins RXD1, EXTINT0, or EXTINT1 can also be used to wake up the receiver from Sleep- or Backup Mode.

2.4.1.1 PIO23

It is a requirement that pin PIO23 is connected to GND.

Always connect PIO23 to GND!

2.4.1.2 PIO21/SCK

Pin PIO21 is shared with the SPI clock pin SCK. PIO21 must be connected to GND if the SPI interface is not used. To use the SPI interface PIO21 must be pulled to a low level during startup. This can be done with a 10k Ohm pull down resistor to GND, see Figure 16. PIO21 must not be left open.

If SPI isn’t used, connect PIO21/SCK to GND.

2.4.1.3 TX Ready (ROM7.03 and above)

The TX ready signal indicates that the receiver has data to transmit. A listener can wait on the TX ready signal instead of polling the DDC or SPI interfaces. The UBX-CFG-PRT message lets you configure the polarity and the number of bytes in the buffer before the TX ready signal goes active. The TX ready signal can be mapped to GPIO 05 (TXD1). The TX ready pin is disabled by default.

Most u-blox wireless modules configure and enable the TX ready functionality automatically at GPIO 05 (TXD1) of AMY-6M. See datasheet of the wireless module.

For more information on configuration and remap of this pin see the AMY-6M Data Sheet [1] and see also the u-blox 6 Receiver Description including Protocol Specification [2].

2.4.2 SAFEBOOT_N

Design a test point to access SAFEBOOT_N in the PCB design. If SAFEBOOT_N is low at start-up, the receiver starts in a Safe Boot Mode and the GPS navigation engine is not started. This mode can be used for production test.

Safe Boot Mode can be used to force the system into a known state regardless of any configuration pins or contents of non-volatile memories. This can be used to recover from a situation where a non-volatile memory was programmed with wrong settings. Since in Safe Boot Mode only a limited number of configurations are available the same restriction may apply as mentioned before with regards to un-programmed non-volatile memory, i.e. baud rates may be wrong or USB may not be functional.

Have at least one test-point available that allows setting pin SAFEBOOT_N to GND. This recommendation should always be followed if external non-volatile memory is used in the application.
2.5 System Configuration

2.5.1 Configuration at start-up

At start-up, the configuration of the system is performed in two steps: First the so-called Low Level Configuration is applied, and then the Functional Configuration is carried out. In between those two steps, the non-volatile memories are detected. See Figure 19 for an overview.

![Figure 19: Configuration at start-up](image)

2.5.1.1 Low Level Configuration

The Low Level Configuration provides some basic configuration information such as GPS mode or reference clock frequency. This information can be supplied in different ways. However, not all of them are available in every setup. The options are:

- **ROM Defaults**: Default settings of the integrated ROM Code. See AMY-6M Data Sheet [1].
- **CFG Pins**: The settings of CFG_COM0/MOSI and CFG_COM1/MISO during boot sequence.

![Figure 20: Low level configuration sequence](image)
2.5.1.2 Functional Configuration

After the Low Level Configuration has been applied the Functional Configuration is executed. The Functional Configuration offers a wide range of information like the configuration of the ports and the messages, the navigation engine settings and the NMEA protocol configuration. This information can be stored on the following non-volatile memories:

- On-chip battery backed RAM (BBR), (V_BCKP supplied by backup battery)
- External serial EEPROM, connected to the DDC (Section 2.3.3.1)
- External serial FLASH memory, connected to the SPI (Section 2.3.4.1)

Figure 21: Functional Block Configuration Sequence

Figure 21 shows the sequence of the Functional Configuration.
2.5.2 Configuration at runtime

Once the receiver has started, the Functional Configuration may be modified with UBX configuration messages. The modified settings remain effective until power-down or reset. If these settings have been stored in non-volatile memory as the EEPROM at DDC or the serial FLASH at SPI, the modified configuration will be retained. If these settings have been stored in battery-backup RAM, then the modified configuration will be retained, as long as the backup battery supply is not interrupted. See chapter “Receiver Configuration” in the u-blox 6 Receiver Description including Protocol Specification [2] for more information.

The configuration pins (CFG_COM0 and CFG_COM1) are shared with other functions (SPI interface pins MOSI and MISO). During start-up, the module first reads the state of the configuration pins. Afterwards the other functions can be used.

For more information about settings and messages see the AMY-6M Data Sheet [1].

2.6 RTC

The RTC crystal is optional as it is only required in stand-alone applications where hot or warm starts are enabled. In these cases, actual time is maintained in the RTC and Ephemeris and other last known data is kept in the backup RAM. In A-GPS based systems, the RTC is not required and coarse or fine time information is available from the network. If neither backup RAM nor RTC are required, V_BCKP should be connected to GND.

The external circuit for normal RTC operation is shown in Figure 2.

If the RTC is not used, its input XTAL_IN should be connected to GND and the output XTAL_OUT must be left open.

As an alternative to the RTC, a 32 kHz signal can be supplied from an external source (e.g. from the host system) into XTAL_IN. This is a core domain signal; its high level must not exceed VDD_B (1.2V!). If the output buffer of the RCT signal from host does exceed the VDD_B voltage, with a voltage divider (Rx and Ry) the voltage level can be adjusted, see Figure 22. Minimum “high” level should be more than 0.8V.

Figure 22: RTC supplied by external source

RTC is highly recommended for Power Save Mode.

If AssistNow Autonomous is required, RTC is mandatory if the time at wakeup of receiver is not provided by message (UBX-AID-INI). For more details see u-blox 6 Receiver Description including Protocol Specification [2].
2.7 RF input

The AMY-6M RF input is already matched to 50 Ohms and has an internal DC block, see Figure 1. To achieve the performance values as written in AMY-6M Data Sheet [1] an active antenna with a good LNA inside or the mandatory LNA in front of AMY-6M must have below 1dB noise figure.

2.7.1 Active Antenna used

In case an active antenna is used, just the active antenna supply circuit has to be added in front of AMY-6M RF-input. See section 2.1.11. In case the active antenna has to be supervised, the Active Antenna Supervisor circuit, see section 2.8, has to be added to the active antenna circuit. This Active Antenna Supervisor circuit also makes sure the active antenna is turned off in some Power Save Mode stages.

2.7.2 Passive Antenna

In case no active antenna is connected to the AMY-6M it is mandatory to use an additional LNA in front of AMY-6M. An LNA (LNA1) alone would make the AMY-6M more sensitive to outband jammers, so an additional GPS SAW filter (F2) has to be connected between the external LNA (LNA1) and the AMY-6M RF-input.

![Figure 23: Recommended passive antenna design](image)

PIO17 can be configured as ANTOFF (active antenna off) signal which can be used to turn off an external LNA. The ANTOFF signal must be inverted for common LNAs which come with an enable pin which has be “low” to turn off. To configure PIO17 as ANTOFF, see u-blox 6 Receiver Description including Protocol Specification [2].

2.7.3 Increased Jamming Immunity

If strong outband jammers are close to the GPS antenna (e.g. a GSM antenna) GPS performance can be decreased or the maximum input power of the AMY-6M RF-input can be exceeded. An additional SAW filter has to put in front of the external LNA (LNA1). If the external LNA (LNA1) can accept the maximum input power, the SAW filter between the passive antenna and external LNA (LNA1) might not be necessary. This results in a better noise figure than an additional SAW filter in front of the external LNA (LNA1).

![Figure 24: Recommended circuit for increased jamming immunity](image)
2.8 Active antenna supervisor

u-blox 6 firmware supports an active antenna supervisor circuit, which can be connected to AMY-6M via pins PIO08/EXTINT1, PIO17, and PIO18. The external components shown in Figure 25 detect whether an active antenna is connected, i.e. if the DC supply current exceeds a threshold defined by R34, R38, and R39, or if a short circuit of the antenna supply has occurred. It will shut down the antenna via transistor T31 if it’s not needed or if a short circuit has been detected.

![Figure 25: Active antenna supervisor circuit](image)

**Equation 1 Calculation of antenna supervisor current (I\text{ANT})**

\[
\frac{V_{\text{ANT}}}{R_{34}} \frac{R_{38}}{R_{39}} = I_{\text{ANT}}
\]

Equation 1 shows the calculation of the antenna supervisor current \(I_{\text{ANT}}\). In case antenna supply voltage \(V_{\text{ANT}}\) exceeds \(VDD\_IO\), open drain buffers U32 (e.g. Fairchild NC7WZ07) and resistors R31 and R30 are required to maintain control on T31 as well as to avoid leakage currents into the internal pull-ups of pins PIO8/EXTINT1 and PIO18.

R34 serves as a current limiter in case of a short circuit.

The three I/Os used for the Antenna Supervisor function are assigned using protocol messages. See u-blox 6 Receiver Description including Protocol Specification [2]

Table 7 shows the functions of the antenna supervisor pins.

<table>
<thead>
<tr>
<th>Function</th>
<th>Input/Output</th>
<th>Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Antenna off</td>
<td>Output</td>
<td>PIO17</td>
</tr>
<tr>
<td>Antenna detection</td>
<td>Input</td>
<td>PIO08/EXTINT1</td>
</tr>
<tr>
<td>Antenna short circuit detection</td>
<td>Input</td>
<td>PIO18</td>
</tr>
</tbody>
</table>

*Table 7: Assignments of the antenna supervisor function*
2.9 Use RESET input

AMY-6M doesn’t come with a RESET_N pin. However, a RESET_N input pin functionality can be implemented by adding a 3k3 resistor in the line to V_RESET, which usually supervises the RF part supply, see Figure 26. Then by driving this Reset input “low” with an open drain buffer, the system is held in a reset state.

Don’t drive this Reset input high! Only drive low or with high impedance (open drain output device). The open drain buffer connected to the Reset input signal must be able to draw around 1mA to GND. Do not use a higher value than 3k3 Ohm, otherwise the V_RESET threshold will be affected.

Figure 26: Reset input circuit for a single 3V power supply design
2.10 Design-in checklist

2.10.1 Schematic design-in checklist for AMY-6M

Check power supply requirements and schematic:

- Is the power supply voltage within the specified range? See how to connect power in Section 2.1.
- For USB devices: Is the voltage VDDUSB voltage within the specified range? Do you have a Bus or Self powered setup?
- Compare the peak current consumption of AMY-6M with the specification of your power supply.
- GPS receivers require a stable power supply. Avoid series resistance in your power supply line (the line to V_DCDC) to minimize the voltage ripple on V_DCDC and VDD_3V.

Backup battery

- For achieving a minimal Time To First Fix (TTFF) after a power down (warmstarts, hotstarts), make sure to connect a backup battery to V_BCKP, and use an RTC. If not used, make sure V_BCKP is connected to GND.

Antenna/RF input

- The total noise figure including external LNA (or the LNA in the active antenna) should be around 1dB.
- With AMY-6M an external LNA is mandatory if no active antenna is used.
- Make sure the antenna is not placed close to noisy parts of the circuitry and not facing noisy parts. (e.g. micro-controller, display, etc.)
- To optimize performance in environments with out-band jamming/interference sources, use an additional SAW filter.

For more information dealing with interference issues see the GPS Antenna Application Note [3].

Schematic

- Pins C9 (PIO21) and E8 (PIO23) must be connected to GND. If SPI is used PIO23 should have a 10k Ohm pull down resistor.
- V_RESET connected to VDD_3V.
- For a 3V single power supply connect V_TH to GND.

2.10.2 AMY-6M design

For a minimal Design with AMY-6M the following functions and pins need to be considered:

- Connect the Power supply to V_DCDC, VDD_IO, VDD_3V, V_BCKP.
- VDDUSB: Connect the USB power supply to a LDO before feeding it to VDDUSB and V_DCDC or connect to GND if USB is not used.
- Ensure an optimal ground connection to all ground pins of the AMY module
- Choose the required serial communication interface (USART, USB, SPI or DDC) and connect the appropriate pins to your application
- If you need Hot- or Warmstart in your application, connect a Backup Battery to V_BCKP and add RTC circuit.
- If antenna bias is required see section 2.1.11.
2.10.3 Minimal schematic for AMY-6M
This is a minimal schematic for a PVT GPS receiver with an AMY-6M module. It is a 3V main supply design (2.5...3.6V) for an active antenna running with main supply voltage. Also Backup part is supplied and RTC connected. Thus Warmstarts and Hotstarts are supported. Communication is UART with main supply voltage levels. Default messages and baudrate are chosen.

Figure 27: Typical schematic of a 3V design for an active antenna (not shown pins have to be left open)
2.10.3.1 Pin description for AMY-6M design

<table>
<thead>
<tr>
<th>Standard Function</th>
<th>I/O</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1 RF_IN</td>
<td>I</td>
<td>RF Input</td>
<td>Add external LNA and SAW if no active antenna used.</td>
</tr>
<tr>
<td>A2 GND</td>
<td>I</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>A3 NC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A4 GND</td>
<td>I</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>A5 XTL_OUT</td>
<td>O</td>
<td>RTC Output</td>
<td>Leave open if no RTC Crystal attached.</td>
</tr>
<tr>
<td>A6 XTL_IN</td>
<td>I</td>
<td>RTC Input</td>
<td>Connect to GND if no RTC Crystal attached.</td>
</tr>
<tr>
<td>A7 VDD_LNA</td>
<td>O</td>
<td>LNA Power Supply</td>
<td>Leave open.</td>
</tr>
<tr>
<td>A8 VDD_ANA</td>
<td>O</td>
<td>Analog Power</td>
<td>Leave open.</td>
</tr>
<tr>
<td>A9 VDD_RF</td>
<td>I/O</td>
<td>Core Power</td>
<td>See section 2.1</td>
</tr>
<tr>
<td>B1 GND</td>
<td>I</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>B2 GND</td>
<td>I</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>B3 Reserved</td>
<td>I/O</td>
<td>Reserved</td>
<td>Do not connect. Must be left open!</td>
</tr>
<tr>
<td>B4 GND</td>
<td>I</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>B5 GND</td>
<td>I</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>B6 GND</td>
<td>I</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>B7 V_TH</td>
<td>I</td>
<td>V_RESET Threshold</td>
<td>Leave open or connect to GND. See section 2.1</td>
</tr>
<tr>
<td>B8 GND</td>
<td>I</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>B9 VDD_USB</td>
<td>I</td>
<td>USB Interface Power</td>
<td>Connect to GND if not used.</td>
</tr>
<tr>
<td>C1 PIO8 / EXTINT1</td>
<td>I</td>
<td>External Interrupt / Alternative function</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>C2 Reserved</td>
<td>I/O</td>
<td>Reserved</td>
<td>Do not connect. Must be left open!</td>
</tr>
<tr>
<td>C7 USB_DM</td>
<td>I/O</td>
<td>USB data</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>C8 PIO18</td>
<td>I</td>
<td>Alternative function, see 2.8</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>C9 PIO21 / SPI SCK</td>
<td>I/O</td>
<td>Reserved / SPI Clock</td>
<td>Must be connected to GND if SPI is not used!</td>
</tr>
<tr>
<td>D1 PIO7 / EXTINT0</td>
<td>I</td>
<td>External Interrupt / Time Mark</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>D2 Reserved</td>
<td>I/O</td>
<td>Reserved</td>
<td>Do not connect. Must be left open!</td>
</tr>
<tr>
<td>D7 USB_DP</td>
<td>I/O</td>
<td>USB data</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>D8 V_RESET</td>
<td>I</td>
<td>Supply Monitor</td>
<td>Connect to VDD_3V. See section 2.1</td>
</tr>
<tr>
<td>D9 VDD_3V</td>
<td>I</td>
<td>Main RF Supply</td>
<td>See section 2.1</td>
</tr>
<tr>
<td>E1 Reserved</td>
<td>I</td>
<td>Reserved</td>
<td>Do not connect. Must be left open!</td>
</tr>
<tr>
<td>E2 Reserved</td>
<td>I</td>
<td>Reserved</td>
<td>Do not connect. Must be left open!</td>
</tr>
<tr>
<td>E8 PIO23</td>
<td>I/O</td>
<td>Reserved</td>
<td>Always connect to GND!</td>
</tr>
<tr>
<td>E9 VDD_B</td>
<td>O</td>
<td>Backup Power</td>
<td>Leave open.</td>
</tr>
<tr>
<td>F1 TIMEPULSE</td>
<td>O</td>
<td></td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>F2 GND</td>
<td>I</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>F3 PIO17</td>
<td>I/O</td>
<td>Alternative function, see 2.7 and 2.8</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>F4 CFG_COM0 / MOSI</td>
<td>I/O</td>
<td>Configuration Pin / SPI MOSI</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>F5 CFG_COM1 / MISO</td>
<td>I/O</td>
<td>Configuration Pin / SPI MISO</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>F6 SS_N</td>
<td>I/O</td>
<td>SPI Chip Select</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>F7 Reserved</td>
<td>I/O</td>
<td>Reserved</td>
<td>Do not connect. Must be left open!</td>
</tr>
<tr>
<td>F8 GND</td>
<td>I</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>F9 V_DCDC</td>
<td>I</td>
<td>Main Core Supply</td>
<td>1.4-3.6V</td>
</tr>
<tr>
<td>G1 VDD_IO</td>
<td>I</td>
<td>I/O Supply</td>
<td>1.65-3.6V</td>
</tr>
<tr>
<td>G2 SAFEBOOT_N</td>
<td>I</td>
<td>Boot Mode Selection</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>G3 SCL2</td>
<td>I/O</td>
<td>DDC for peripherals</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>G4 SDA2</td>
<td>I/O</td>
<td>DDC for peripherals</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>G6 TxD1</td>
<td>O</td>
<td>Asynchronous Serial</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>G6 RxD1</td>
<td>I</td>
<td>Asynchronous Serial</td>
<td>Leave open if not used.</td>
</tr>
<tr>
<td>G7 V_BCKP</td>
<td>I</td>
<td>Backup voltage supply</td>
<td>1.4-3.6V (optional). Connect to GND if not used.</td>
</tr>
<tr>
<td>G8 VDD_C</td>
<td>O</td>
<td>Core Power</td>
<td>Leave open.</td>
</tr>
<tr>
<td>G9 DCDC_EN</td>
<td>O</td>
<td>Enable for external DCDC-converter</td>
<td>Leave open if not used.</td>
</tr>
</tbody>
</table>

Table 8: Pinout AMY-6M
2.11 Layout design-in checklist

Follow this checklist for the layout design to get an optimal GPS performance.

**Layout optimizations (Section 2.12)**

- Is the AMY-6M placed according to the recommendation in Section 2.12.3?
- Is the Grounding concept optimal?
- Has the 50 Ohm line from antenna to AMY-6M (micro strip/coplanar waveguide) been kept as short as possible?
- Assure low serial resistance in V_DCDC power supply line (choose a line width >400um)
- Keep power supply line as short as possible
- Design a GND guard ring around the optional RTC crystal lines and GND below the RTC circuit.
- Add a ground plane underneath the GPS module to reduce interference. Especially for the RF input line.
- For improved shielding, add as many vias as possible around the micro strip/coplanar waveguide, around the serial communication lines, underneath the GPS module etc.

**Calculation of the micro strip for RF input**

- The micro strip/coplanar waveguide must be 50 Ohms and be routed in a section of the PCB where minimal interference from noise sources can be expected. Make sure around the RF line is only GND as well as under the RF line.
- In case of a multi-layer PCB, use the thickness of the dielectric between the signal and the 1st GND layer (typically the 2nd layer) for the micro strip/coplanar waveguide calculation.
- If the distance between the micro strip and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the “Coplanar Waveguide” model in AppCad to calculate the micro strip and not the “micro strip” model.
2.12 Layout

This section provides important information for designing a reliable and sensitive GPS system.

GPS signals at the surface of the Earth are about 15dB below the thermal noise floor. Signal loss at the antenna and the RF connection must be minimized as much as possible. When defining a GPS receiver layout, the placement of the antenna with respect to the receiver, as well as grounding, shielding and jamming from other digital devices are crucial issues and need to be considered very carefully.

2.12.1 Footprint

Figure 28: Recommended footprint (top view)

Units in are in mm.

2.12.2 Paste mask

The paste mask shall be 50µm smaller than the copper pads with a paste thickness of 100µm.

These are recommendations only and not specifications. The exact geometry, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

2.12.3 Placement

A very important factor in achieving maximum GPS performance is the placement of the receiver on the PCB. The connection to the antenna must be as short as possible to avoid jamming into the very sensitive RF section. Make sure that RF critical circuits are clearly separated from any other digital circuits on the system board. To achieve this, position the receiver digital part towards your digital section of the system PCB. Care must also be
exercised with placing the receiver in proximity to circuitry that can emit heat. The RF part of the receiver is very sensitive to temperature and sudden changes can have an adverse impact on performance.

**AMY-6M receivers are temperature sensitive devices. Avoid high temperature drift and air vents near the receiver.**

### 2.13 Migration considerations

The main difference between u-blox AMY-5M and u-blox AMY-6M from migration point of view is that the 3 pins EXTINT0 (PIO7), EXTINT1 (PIO8) and RXD1 (PIO4) have moved from the backup (VDD_B) domain to the IO (VDD_IO) domain and these 3 pins now have an internal pull-up to VDD_IO. As a consequence the following things must be considered when migrating from an existing u-blox 5 design to u-blox 6.

The external series resistors in the USB_DM nd USB_DP lines have changed from 27 Ohm to now 22 Ohm.

- Change series resistors in USB_DM and USB_DP line to 22 Ohm
- The signal levels for RxD1, EXTINT0 and EXTINT1 are now related to VDD_IO and have the same input levels as all the other IOs. There is no longer any exception for the signal input levels for RxD1, EXTINT0 or EXTINT1.
- External pull-ups or pull-downs at RxD1, EXTINT0 and EXTINT1 must be removed. u-blox AMY-6M has internal pull-ups to VDD_IO at RxD1, EXTINT0 and EXTINT1.
- If RxD1, EXTINT0 and EXTINT1 were connected to GND on the u-blox 5 design, this will result in increased current for u-blox 6 in SW backup mode. For example if VDD_IO is 3 V, RxD1 is used for communication and EXTINT0/EXTINT1 are connected to GND, then there will be an increased current of about \(2 \times \frac{VDD_IO}{pullup} = 2 \times \frac{3 V}{113 k\text{Ohm}} = 53 \mu\text{A} \).  

**For u-blox 5 designs with RxD1, EXTINT0 or EXTINT1 connected directly to VDD_B, the layout cannot be directly migrated to u-blox AMY-6M and must be modified.**
2.14 EOS/ESD/EMI precautions

When integrating GPS receivers into wireless systems, careful consideration must be given to electromagnetic and voltage susceptibility issues. Wireless systems include components which can produce Electrostatic Discharge (ESD), Electrical Overstress (EOS) and Electro-Magnetic Interference (EMI). CMOS devices are more sensitive to such influences because their failure mechanism is defined by the applied voltage, whereas bipolar semiconductors are more susceptible to thermal overstress. The following design guidelines are provided to help in designing robust yet cost effective solutions.

- To avoid overstress damage during production or in the field it is essential to observe strict EOS/ESD/EMI handling and protection measures.
- To prevent overstress damage at the RF_IN of your receiver, never exceed the maximum input power as specified in AMY-6M Data Sheet [1].

2.14.1 Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSI</td>
<td>American National Standards Institute</td>
</tr>
<tr>
<td>CDMA</td>
<td>Code Division Multiple Access</td>
</tr>
<tr>
<td>EMC</td>
<td>Electromagnetic compatibility</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic interference</td>
</tr>
<tr>
<td>EOS</td>
<td>Electrical Overstress</td>
</tr>
<tr>
<td>EPA</td>
<td>Electrostatic Protective Area</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic discharge</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>GPS</td>
<td>Global Positioning System</td>
</tr>
<tr>
<td>GSM</td>
<td>Global System for Mobile Communications</td>
</tr>
<tr>
<td>IEC</td>
<td>International Electrotechnical Commission</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed circuit board</td>
</tr>
</tbody>
</table>

Table 9: Explanation of abbreviations used in this section

2.14.2 Electrostatic Discharge (ESD)

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

2.14.3 ESD protection measures

- GPS receivers are sensitive to Electrostatic Discharge (ESD). Special precautions are required when handling.

Most defects caused by ESD can be prevented by following strict ESD protection rules for production and handling. When implementing passive antenna patches or external antenna connection points, then additional ESD measures as shown in Figure 29 can also avoid failures in the field.
2.14.4 Electrical Overstress (EOS)

Electrical Overstress (EOS) usually describes situations when the maximum input power exceeds the maximum specified ratings. EOS failure can happen if RF emitters are close to a GPS receiver or its antenna. EOS causes damage to the chip structures.

If the RF_IN is damaged by EOS, it’s hard to determine whether the chip structures have been damaged by ESD or EOS.

2.14.5 EOS protection measures

EOS protection measures as shown in Figure 30 are recommended for any designs combining wireless communication transceivers (e.g. GSM, GPRS) and GPS in the same design or in close proximity.

2.14.6 Electromagnetic Interference (EMI)

Electromagnetic interference (EMI) is the addition or coupling of energy released from any RF emitting device. This can cause a spontaneous reset of the GPS receiver or result in unstable performance. Any unshielded line or segment (>3mm) connected to the GPS receiver can effectively act as an antenna and lead to EMI disturbances or damage.

The following elements are critical regarding EMI:
- Unshielded connectors (e.g. pin rows etc.)
- Weakly shielded lines on PCB (e.g. on top or bottom layer and especially at the border of a PCB)
- Weak GND concept (e.g. small and/or long ground line connections)

EMI protection measures are recommended when RF emitting devices are near the GPS receiver. To minimize the effect of EMI a robust grounding concept is essential. To achieve electromagnetic robustness follow the standard EMI suppression techniques.


Improved EMI protection can be achieved by inserting a resistor or better yet a ferrite bead (BLM15HD102SN1) into any unshielded PCB lines connected to the GPS receiver. Place the resistor as close as possible to the GPS receiver pin.

Example of EMI protection measures on the RX/TX line using a ferrite bead:

![Figure 31: EMI Precautions](image)

VCC can be protected using a feed thru capacitor. For electromagnetic compatibility (EMC) of the RF_IN pin refer to section 2.14.5

2.14.7 GSM applications

GSM uses power levels up to 2W (+33dBm). Make sure that absolute maximum input power level of GPS receiver is not exceeded. See AMY-6M Data Sheet [1].

2.14.7.1 Isolation between GPS and GSM antenna

In a handheld type design an isolation of approximately 20dB can be reached with careful placement of the antennas. If such isolation can’t be achieved, e.g. in the case of an integrated GSM/GPS antenna, an additional input filter is needed on the GPS side to block the high energy emitted by the GSM transmitter. Examples of these kinds of filters would be the SAW Filters from Epcos (B9444 or B7839) or Murata.

2.14.7.2 Increasing interference immunity

Interference signals come from in-band and out-band frequency sources.

2.14.7.3 In-band interference

With in-band interference the signal frequency is very close to the GPS frequency of 1575 MHz (see Figure 32). Such interference signals are typically caused by harmonics from displays, micro-controller, bus systems, etc.
Measures against in-band interference include:
- Maintaining a good grounding concept in the design
- Shielding
- Layout optimisation
- Filtering
- Placement of the GPS antenna
- Adding a CDMA, GSM, WCDMA bandbass filter before handset antenna

2.14.7.4 Out-band interference
Out-band interference is caused by signal frequencies that are different from the GPS carrier (see Figure 34). The main sources are wireless communication systems such as GSM, CDMA, WCDMA, WiFi, BT, etc..

Figure 32: In-band interference signals

Figure 33: In-band interference sources

Figure 34: Out-band interference signals
Measures against out-band interference include maintaining a good grounding concept in the design and adding a SAW or bandpass ceramic filter (as recommend in Section 2.14.5) into the antenna input line to the GPS receiver (see Figure 35).

![Figure 35: Measures against out-band interference](image)

### 2.14.8 Recommended parts

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Part ID</th>
<th>Remarks</th>
<th>Parameters to consider</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode</td>
<td>ES9DR3.3ST5G</td>
<td>(2.14.3 B) Standoff Voltage&gt;3.3V</td>
<td>• Low Capacitance &lt; 0.5pF</td>
</tr>
<tr>
<td></td>
<td>ES9DL3.3ST5G</td>
<td>(2.14.3 B) Standoff Voltage&gt;3.3V</td>
<td>• Standoff Voltage &gt; Voltage for active antenna</td>
</tr>
<tr>
<td></td>
<td>ES9DL5.0ST5G</td>
<td>(2.14.3 B) Standoff Voltage&gt;5V</td>
<td>• Low Inductance</td>
</tr>
<tr>
<td>SAW</td>
<td>B9444: B39162-B9444-M410</td>
<td>(2.14.5) 15dBm Max Power</td>
<td>• Low-loss RF filter for GPS</td>
</tr>
<tr>
<td></td>
<td>B7839: B39162-B7839-K410</td>
<td>(2.14.5) 25dBm Max Power</td>
<td>• Unbalanced to unbalanced operation</td>
</tr>
<tr>
<td></td>
<td>SAFE1G57KD0F00</td>
<td>(2.14.5)</td>
<td>• Insertion Loss</td>
</tr>
<tr>
<td></td>
<td>SAF3E1G57KA0790</td>
<td>(2.14.5) 2.5x2.0x1.0 mm</td>
<td>• Bandwidth and BW over temperature</td>
</tr>
<tr>
<td></td>
<td>CER0032A</td>
<td>(2.14.5) 4.2x4.0x2.0 mm</td>
<td>• Electrostatic Sensitive Device (ESD MM)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&gt; 8kV ESD HBM</td>
<td>• SiGe (pHEMT (GaAS))</td>
</tr>
<tr>
<td>LNA</td>
<td>ALM-1106</td>
<td>(2.14.3 A)</td>
<td>LNA</td>
</tr>
<tr>
<td></td>
<td>ALM-1412</td>
<td>(2.14.3 C)</td>
<td>LNA + FBAR Filter</td>
</tr>
<tr>
<td></td>
<td>ALM-1712</td>
<td>(2.14.5)</td>
<td>Filter + LNA + FBAR Filter</td>
</tr>
<tr>
<td></td>
<td>ALM-2412</td>
<td>(2.14.3 A)</td>
<td>LNA + FBAR Filter</td>
</tr>
<tr>
<td>Capacitor</td>
<td>GRM1555C1E470JZ01</td>
<td>(2.14.5 D)</td>
<td>C, 47p</td>
</tr>
<tr>
<td>Ferrite Bead</td>
<td>BLM15HD1025N1</td>
<td>(2.14.5 D)</td>
<td>FB</td>
</tr>
<tr>
<td>Feed thru Capacitor for Signal</td>
<td>NFL18SP157X1A3</td>
<td>Monolithic Type</td>
<td>Load Capacitance appropriate to Baude rate</td>
</tr>
<tr>
<td></td>
<td>NFA18SL307V1A45</td>
<td>Array Type</td>
<td>CL &lt; xxx pF</td>
</tr>
<tr>
<td>Feed thru Capacitor for VCC</td>
<td>NFM18PC</td>
<td>0603 2A</td>
<td>Rs &lt; 0.5 Ohm</td>
</tr>
<tr>
<td></td>
<td>NFM21P</td>
<td>0805 4A</td>
<td></td>
</tr>
</tbody>
</table>

**Table 10: Recommended parts for ESD/EOS protection**
3 Product handling & soldering

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to reels and tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning see the AMY-6M Data Sheet [1].

3.2 ESD handling precautions

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials in the vicinity of ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

GPS receivers are sensitive to ESD and require special precautions when handling. Particular care must be exercised when handling patch antennas, due to the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the receiver.

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB shall always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device.
- When handling the RF pin, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10pf, coax cable ~50-80pf/m, soldering iron, …)

- To prevent electrostatic discharge through the RF input, do not touch the mounted patch antenna.

- When soldering RF connectors and patch antennas to the receiver's RF pin, make sure to use an ESD safe soldering iron (tip).

⚠️ Failure to observe these precautions can result in severe damage to the GPS receiver!

3.3 Soldering

3.3.1 Soldering paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place.

Stencil Thickness: 100 to 150 µm for base boards

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.12.2
3.3.2 Reflow soldering

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preheat/Soak Temperature min.</td>
<td>T_{\text{min}}</td>
</tr>
<tr>
<td>Preheat/Soak Temperature max.</td>
<td>T_{\text{max}}</td>
</tr>
<tr>
<td>Preheat/Soak Time from T_{\text{min}} to T_{\text{max}}</td>
<td>t_{\text{pre}}</td>
</tr>
<tr>
<td>Liquidus Temperature</td>
<td>T_{L}</td>
</tr>
<tr>
<td>Time maintained above T_{L}</td>
<td>t_{L}</td>
</tr>
<tr>
<td>Peak Package Body Temperature</td>
<td>T_{P}</td>
</tr>
<tr>
<td>Ramp up rate (T_{L} to T_{P})</td>
<td>3°C/second max.</td>
</tr>
<tr>
<td>Time within +0°C…-5°C of T_{P}</td>
<td>30 seconds</td>
</tr>
<tr>
<td>Ramp down rate (T_{P} to T_{L})</td>
<td>4°C/second max.</td>
</tr>
</tbody>
</table>

Table 11: Recommended conditions for reflow process

The peak temperature must not exceed 250°C. The time above 245°C must not exceed 30 seconds.

AMY-6M must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the AMY-6M module, consider an optical inspection step to check whether:

- The module is properly aligned and centered over the pads

3.3.4 Repeated reflow soldering

Only single reflow soldering processes are recommended for boards populated with AMY-6M modules.

3.3.5 Wave soldering

Base boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with AMY-6M.

3.3.6 Rework

Not recommended.

3.3.7 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

Conformal Coating of the module will void the warranty.

3.3.8 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the u-blox 6 module before implementing this in the production.

Casting will void the warranty.

3.3.9 Use of ultrasonic processes

Some components on the u-blox 6 module are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the GPS Receiver.

u-blox offers no warranty against damages to the u-blox 6 module caused by any Ultrasonic Processes.
3.4 Safety precautions

AMY-6M modules must be supplied by an external limited power source in compliance with the clause 2.5 of the standard IEC 60950-1. In addition to an external limited power source, only separated or Safety Extra-Low Voltage (SELV) circuits are to be connected to the module, including interfaces and antennas.

For more information about SELV circuits, see section 2.2 in Safety standard IEC 60950-1 [6].
4 Product testing

4.1 Test parameters for OEM manufacturer

Because of the testing done by u-blox, it is obvious that an OEM manufacturer doesn’t need to repeat firmware tests or measurements of the GPS parameters/characteristics (e.g. TTFF) in their production test.

An OEM manufacturer should focus on:
- Overall sensitivity of the device (including antenna, if applicable)
- Communication to a host controller

4.2 System sensitivity test

The best way to test the sensitivity of a GPS device is with the use of a 1-channel GPS simulator. It assures reliable and constant signals at every measurement.

u-blox recommends the following Single-Channel GPS Simulator:
- Spirent GSS6100
  Spirent Communications Positioning Technology
  www.positioningtechnology.co.uk

4.2.1 Guidelines for sensitivity tests

1. Connect a 1-channel GPS simulator to the OEM product
2. Choose the power level in a way that the “Golden Device” would report a C/No ratio of 38-40 dBHz
3. Power up the DUT (Device Under Test) and allow enough time for the acquisition
4. Read the C/No value from the NMEA GSV or the UBX-NAV-SVINFO message (e.g. with u-center)
5. Compare the results to a “Golden Device” or a u-blox 6 Evaluation Kit.

4.2.2 ‘Go/No go’ tests for integrated devices

The best test is to bring the device to an outdoor position with excellent sky view (HDOP < 3.0). Let the receiver acquire satellites and compare the signal strength with a “Golden Device”.

As the electro-magnetic field of a redistribution antenna is not homogenous, indoor tests are in most cases not reliable. These kind of tests may be useful as a ‘go/no go’ test but not for sensitivity measurements.
## A Migration to u-blox 6 receivers

### A.1 Migration from AMY-5M to AMY-6M

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Typical Assignment</th>
<th>Pin Name</th>
<th>Typical Assignment</th>
<th>Remarks for Migration</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1 RF_IN</td>
<td>RF_IN</td>
<td>A2 GND</td>
<td>GND</td>
<td>no change</td>
</tr>
<tr>
<td>A3 NC</td>
<td>NC</td>
<td>A4 GND</td>
<td>GND</td>
<td>no change</td>
</tr>
<tr>
<td>A5 XTAL_OUT</td>
<td>Leave open if no RTC attached.</td>
<td>A6 XTAL_IN</td>
<td>GND if no RTC attached.</td>
<td>no change</td>
</tr>
<tr>
<td>A7 VDD_LNA</td>
<td>Supply capacitor to GND.</td>
<td>A8 VDD_ANA</td>
<td>Supply capacitor to GND.</td>
<td>No need to populate capacitor.</td>
</tr>
<tr>
<td>A9 VDD_RF</td>
<td>Supply capacitor to GND.</td>
<td>B1 GND</td>
<td>GND</td>
<td>no change</td>
</tr>
<tr>
<td>B2 GND</td>
<td>GND</td>
<td>B3 Reserved</td>
<td>Do not connect.</td>
<td>no change</td>
</tr>
<tr>
<td>B4 GND</td>
<td>GND</td>
<td>B5 GND</td>
<td>GND</td>
<td>no change</td>
</tr>
<tr>
<td>B6 GND</td>
<td>GND</td>
<td>B7 V_TH</td>
<td>V_TH</td>
<td>no change</td>
</tr>
<tr>
<td>B8 GND</td>
<td>GND</td>
<td>B9 VDD_USB</td>
<td>Connect to GND if not used.</td>
<td>no change</td>
</tr>
<tr>
<td>C1 PIO8 / EXTINT1</td>
<td>Pull-up resistor of 100k to VDD.IO.</td>
<td>C2 Reserved</td>
<td>Do not connect.</td>
<td>no change</td>
</tr>
<tr>
<td>C7 USB_DM</td>
<td>Leave open if not used.</td>
<td>C8 PIO18</td>
<td>Leave open</td>
<td>no change</td>
</tr>
<tr>
<td>C9 PIO21</td>
<td>Always connect to GND</td>
<td>C10 PIO23</td>
<td>Always connect to GND</td>
<td>No need to populate resistor. Input voltage levels have changed. See AMY-6M Data Sheet [1].</td>
</tr>
<tr>
<td>D1 PIO7 / EXTINT0</td>
<td>Pull-up resistor of 100k to VDD.IO.</td>
<td>D2 Reserved</td>
<td>Leave open.</td>
<td>no change</td>
</tr>
<tr>
<td>D7 USB_DP</td>
<td>Leave open if not used.</td>
<td>D8 V_Reset</td>
<td>Connect to VDD_3V.</td>
<td>no change</td>
</tr>
<tr>
<td>D9 VDD_3V</td>
<td>VDD_3V</td>
<td>E1 Reserved</td>
<td>Leave open.</td>
<td>no change</td>
</tr>
<tr>
<td>E2 Reserved</td>
<td>Leave open.</td>
<td>E8 PIO23</td>
<td>Always connect to GND.</td>
<td>no change</td>
</tr>
<tr>
<td>E9 VDD_B</td>
<td>NC or supply cap</td>
<td>F1 TIMEPULSE</td>
<td>Leave open if not used.</td>
<td>no change</td>
</tr>
</tbody>
</table>

External series resistor should be changed to 22 Ohm instead of 27 Ohm if USB is used.

See AMY-6M Data Sheet [1].
<table>
<thead>
<tr>
<th>Pin</th>
<th>AMY-5M Pin Name</th>
<th>AMY-5M Typical Assignment</th>
<th>AMY-6M Pin Name</th>
<th>AMY-6M Typical Assignment</th>
<th>Remarks for Migration</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>no change</td>
</tr>
<tr>
<td>F3</td>
<td>PIO17</td>
<td>Leave open</td>
<td>PIO17</td>
<td>Leave open</td>
<td>no change</td>
</tr>
<tr>
<td>F4</td>
<td>PIO19 / CFG_COM0</td>
<td>Leave open if not used</td>
<td>CFG_COM0/ MOSI</td>
<td>Leave open if not used</td>
<td>no change</td>
</tr>
<tr>
<td>F5</td>
<td>PIO20 / CFG_COM1</td>
<td>Leave open if not used</td>
<td>CFG_COM1/ MISO</td>
<td>Leave open if not used</td>
<td>no change</td>
</tr>
<tr>
<td>F6</td>
<td>PIO6</td>
<td>Leave open</td>
<td>SS_N</td>
<td>Leave open if not used</td>
<td>no change</td>
</tr>
<tr>
<td>F7</td>
<td>Reserved</td>
<td>Do not connect</td>
<td>Reserved</td>
<td>Leave open</td>
<td>no change</td>
</tr>
<tr>
<td>F8</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>no change</td>
</tr>
<tr>
<td>F9</td>
<td>V_DCDC</td>
<td>V_DCDC</td>
<td>V_DCDC</td>
<td>V_DCDC</td>
<td>no change</td>
</tr>
<tr>
<td>G1</td>
<td>VDD_IO</td>
<td>1.65-3.6V</td>
<td>VDD_IO</td>
<td>1.65-3.6V</td>
<td>no change</td>
</tr>
<tr>
<td>G2</td>
<td>TDI / SAFEBOOT_N</td>
<td>Leave open if not used.</td>
<td>SAFEBOOT_N</td>
<td>Leave open if not used</td>
<td>no change</td>
</tr>
<tr>
<td>G3</td>
<td>PIO3 / SCL2</td>
<td>Leave open if not used.</td>
<td>SCL2</td>
<td>Leave open if not used</td>
<td>no change</td>
</tr>
<tr>
<td>G4</td>
<td>PIO2 / SDA2</td>
<td>Leave open if not used.</td>
<td>SDA2</td>
<td>Leave open if not used</td>
<td>no change</td>
</tr>
<tr>
<td>G5</td>
<td>PIO5 / TxD1</td>
<td>Leave open if not used.</td>
<td>TxD1</td>
<td>Leave open if not used</td>
<td>no change</td>
</tr>
<tr>
<td>G6</td>
<td>PIO4 / RxD1</td>
<td>Pull-up resistor of 100k to VDD_IO.</td>
<td>RxD1</td>
<td>Leave open if not used.</td>
<td>No need to populate resistor. Input voltage levels have changed. See AMY-6M Data Sheet [1].</td>
</tr>
<tr>
<td>G7</td>
<td>V_BCKP</td>
<td>1.4-3.6V (optional). Connect to GND if not used</td>
<td>V_BCKP</td>
<td>1.4-3.6V. Connect to GND if not used.</td>
<td>no change</td>
</tr>
<tr>
<td>G8</td>
<td>VDD_C</td>
<td>Supply capacitor, required 2.2 µF</td>
<td>VDD_C</td>
<td>Leave open.</td>
<td>No need to populate capacitor.</td>
</tr>
<tr>
<td>G9</td>
<td>NC</td>
<td>Leave open</td>
<td>DCDC_EN</td>
<td>Leave open if not used.</td>
<td>no change</td>
</tr>
</tbody>
</table>
B Component selection

This section provides information about components that are critical for the performance of the AMY-6M GPS receiver module.

Temperature range specifications need only be as wide as required by a particular application. For the purpose of this document, specifications for industrial temperature range (-40 °C ... +85 °C) are provided.

B.1 RTC crystal (Y2)

<table>
<thead>
<tr>
<th>ID</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Frequency Specifications</td>
<td>Fundamental Mode</td>
</tr>
<tr>
<td>1.1</td>
<td>Oscillation mode</td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td>Nominal frequency at 25 °C</td>
<td>32.768 kHz</td>
</tr>
<tr>
<td>1.3</td>
<td>Frequency calibration tolerance at 25 °C</td>
<td>&lt; ±100 ppm</td>
</tr>
<tr>
<td>2</td>
<td>Electrical Specifications</td>
<td></td>
</tr>
<tr>
<td>2.1</td>
<td>Load capacitance C_L</td>
<td>9 pF</td>
</tr>
<tr>
<td>2.2</td>
<td>Equivalent series resistance R_S</td>
<td>50 kΩ</td>
</tr>
</tbody>
</table>

Table 12: RTC Crystal specifications

Manufacturer | Order No.
Micro Crystal | CC7V-T1A 32.768 kHz 9.0 pF +/- 100 ppm

Table 13: Recommend parts list for RTC Crystal Y2

B.2 I2C Serial EEPROM memory

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Order No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST</td>
<td>M24C32-R</td>
</tr>
<tr>
<td>Microchip</td>
<td>24AA32A</td>
</tr>
<tr>
<td>Catalyst</td>
<td>CAT24C32</td>
</tr>
<tr>
<td>Samsung</td>
<td>S524AB0X91</td>
</tr>
</tbody>
</table>

Table 14: Recommend parts list for I2C Serial EEPROM memory

B.3 Serial FLASH Memory

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Order No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Winbond</td>
<td>W25X10A</td>
</tr>
<tr>
<td>Winbond</td>
<td>W25X20A</td>
</tr>
<tr>
<td>AMIC</td>
<td>A25L010</td>
</tr>
<tr>
<td>AMIC</td>
<td>A25L020</td>
</tr>
</tbody>
</table>

Table 15: Recommend parts list for serial FLASH memory

B.4 USB line protection (D2)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Order No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST Microelectronics</td>
<td>USBLCE-2</td>
</tr>
</tbody>
</table>

Table 16: Recommend parts list for USB line protection

B.5 USB LDO (U4)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Order No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Seiko Instruments Inc.</td>
<td>S-1206833-16T2G</td>
</tr>
</tbody>
</table>

Table 17: Recommend parts list for USB LDO
B.6 Operational amplifier (U31)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Order No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear Technology</td>
<td>LT6000</td>
</tr>
<tr>
<td>Linear Technology</td>
<td>LT6003</td>
</tr>
</tbody>
</table>

Table 18: Recommend parts list for operational amplifier

B.7 Dual open-drain buffer (U32)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Order No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fairchild</td>
<td>NC7W07P6X</td>
</tr>
</tbody>
</table>

Table 19: Recommend parts list for dual open-drain buffer

B.8 Antenna supervisor switch transistor (T31)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Order No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vishay</td>
<td>Si1016X-T1-E3</td>
</tr>
</tbody>
</table>

Table 20: Recommend parts list for antenna supervisor switch transistor

B.9 Ferrite bead filter (FB1)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Order No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>muRata</td>
<td>BLM15HD102SN1</td>
</tr>
</tbody>
</table>

Table 21: Recommend parts list for the ferrite bead filter

B.10 Inductor (L)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Order No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>muRata</td>
<td>LQG15HS27NJ02</td>
</tr>
</tbody>
</table>

Table 22: Recommend parts list for inductor

B.11 Standard capacitors

<table>
<thead>
<tr>
<th>Name</th>
<th>Use</th>
<th>Type / Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>RF-input DC block</td>
<td>COG 47P 5% 25V</td>
</tr>
<tr>
<td>C</td>
<td>Decoupling Capacitor</td>
<td>X5R 100N 10% 10V</td>
</tr>
<tr>
<td>C19</td>
<td>Load capacitor XTAL_IN</td>
<td>COG 12P 5% 25V</td>
</tr>
<tr>
<td>C20</td>
<td>Load capacitor XTAL_OUT</td>
<td>COG 12P 5% 25V</td>
</tr>
<tr>
<td>C23</td>
<td>Decoupling capacitor at VBUS</td>
<td>Depends on USB LDO (U3) specification</td>
</tr>
<tr>
<td>C24</td>
<td>Decoupling capacitor at VBUS</td>
<td>Depends on USB LDO (U3) specification</td>
</tr>
</tbody>
</table>

Table 23: Standard capacitors
### B.12 Standard resistors

<table>
<thead>
<tr>
<th>Name</th>
<th>Use</th>
<th>Type / Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>Active antenna supply (VDD_3V)</td>
<td>10R 5% 0.1W</td>
</tr>
<tr>
<td>R4</td>
<td>USB data serial termination</td>
<td>22R 5% 0.1W</td>
</tr>
<tr>
<td>R5</td>
<td>USB data serial termination</td>
<td>22R 5% 0.1W</td>
</tr>
<tr>
<td>R8</td>
<td>Pull-up at RXD1</td>
<td>100k 5% 0.1W</td>
</tr>
<tr>
<td>R9</td>
<td>Pull-up at EXTINT0</td>
<td>100k 5% 0.1W</td>
</tr>
<tr>
<td>R10</td>
<td>Pull-up at EXTINT1</td>
<td>100k 5% 0.1W</td>
</tr>
<tr>
<td>R11</td>
<td>Pull-down at VDD_USB</td>
<td>10K 5% 0.1W</td>
</tr>
<tr>
<td>R30</td>
<td>Pull-up at antenna supervisor transistor</td>
<td>100K 5% 0.1W</td>
</tr>
<tr>
<td>R31</td>
<td>Antenna supervisor input current limiter</td>
<td>39K 5% 0.1W</td>
</tr>
<tr>
<td>R34</td>
<td>Antenna supervisor current limiter</td>
<td>10R 5% 0.25W</td>
</tr>
<tr>
<td>R38</td>
<td>Antenna supervisor voltage divider</td>
<td>560R 5% 0.1W</td>
</tr>
<tr>
<td>R39</td>
<td>Antenna supervisor voltage divider</td>
<td>100K 5% 0.1W</td>
</tr>
</tbody>
</table>

Table 24: Standard resistors

### B.13 LNA (LNA1)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Order No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAXIM</td>
<td>MAX2659ELT+</td>
</tr>
<tr>
<td>JRC</td>
<td>NJG1143UA2</td>
</tr>
</tbody>
</table>

Table 25: recommended LNAs

### B.14 SAW Filter (F2)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Order No.</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>EPCOS</td>
<td>B9415: B39162-B9415-K610</td>
<td>Low insertion loss</td>
</tr>
<tr>
<td>EPCOS</td>
<td>B9444: B39162-B9444-M410</td>
<td>Good wireless band suppression</td>
</tr>
<tr>
<td>MuRata</td>
<td>SAFE1G57KB0F00</td>
<td>Very low insertion loss</td>
</tr>
<tr>
<td>MuRata</td>
<td>SAFE1G57KA0T90</td>
<td></td>
</tr>
<tr>
<td>MuRata</td>
<td>SAFEA1G57KE0F00</td>
<td>Good wireless band suppression</td>
</tr>
<tr>
<td>CTS</td>
<td>CER0032A</td>
<td>Ceramic filter also offers robust ESD Protection</td>
</tr>
<tr>
<td>TriQuint</td>
<td>856561</td>
<td>Compliant to the AEC-Q200 standard</td>
</tr>
</tbody>
</table>

Table 26: recommended SAW Filters
C Interface Backgrounder

C.1 DDC Interface

Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. These lines are connected to all devices on the DDC. SCL is used to synchronize data transfers and SDA is the data line. Both SCL and SDA lines are "open drain" drivers. This means that DDC devices can only drive them low or leave them open. The pull-up resistor (Rp) pulls the line up to \( V_{DD} \) if no DDC device is pulling it down to GND. If the pull-up resistors are missing, the SCL and SDA lines are undefined and the DDC bus will not work. For most DDC systems the low and high input voltage level thresholds of SDA and SCL depend on \( V_{DD} \). See the AMY-6M Data Sheet \([1]\) for the applicable voltage levels.

![Figure 37: A simple DDC connection](image)

The signal shape and the maximum rate in which data can be transferred over SDA and SCL is limited by the values of Rp and the wire and \( V_O \) capacitance (Cp). Long wires and a large number of devices on the bus increase Cp, therefore DDC connections should always be as short as possible. The resistance of the pull-up resistors and the capacitance of the wires should be carefully chosen.

![Figure 38: DDC block diagram](image)

C.1.1 Addresses, roles and modes

Each device connected to a DDC is identified by a unique 7-bit address (e.g. whether it’s a microcontroller, EEPROM or D/A Converter, etc.) and can operate as either a transmitter or receiver, depending on the function of the device. The default DDC address for u-blox GPS receivers is set to 0x42. Setting the mode field in the CFG-PRT message for DDC accordingly can change this address.
The first byte sent is comprised of the address field and R/W bit. Hence the byte seen on the bus 0x42 is shifted by 1 to the left plus R/W bit thus being 0x84 or 0x85 if analyzed by scope or protocol analyzer.

In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave. The DDC-bus is a multi-master bus, i.e. multiple devices are capable of controlling the bus. Such architecture is not permanent and depends on the direction of data transfer at any given point in time. A master device not only allocates the time slots when slaves can respond but also enables and synchronizes designated slaves to physically access the bus by driving the clock. Although multiple nodes can assume the role of a master, only one at any time is permitted to do so. Thus, when one node acts as master, all other nodes act as slaves. Table 27 shows the possible roles and modes for devices connected to a DDC bus.

<table>
<thead>
<tr>
<th>Role</th>
<th>Transmit</th>
<th>Receive</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Master</strong>: sends the clock and addresses slaves</td>
<td>Sends data to slave</td>
<td>Receives data from slave</td>
</tr>
<tr>
<td><strong>Slave</strong>: receives the clock and address</td>
<td>Sends data to master</td>
<td>Receives data from master</td>
</tr>
</tbody>
</table>

Table 27: Possible roles and modes of devices connected to DDC bus

u-blox 6 GPS receivers normally run in the slave mode. There is an exception when an external EEPROM is attached. In that case, the receiver attempts to establish presence of such a non-volatile memory component by writing and reading from a specific location. If EEPROM is present (assumed to be located at a fixed address 0x0A), the receiver assumes the role of a master on the bus and never changes role to slave until the following start-up (subject to EEPROM presence). This process takes place only once at the start-up, i.e. the receiver’s role cannot be changed during the normal operation afterward. This model is an exception and should not be implemented if there are other participants on the bus contending for the bus control (μC / CPU, etc.).

As a slave on the bus, the u-blox 6 GPS receiver cannot initiate the data transfers. The master node has the exclusive right and responsibility to generate the data clock, therefore the slave nodes need not be configured to use the same baud rate. For the purpose of simplification, if not specified differently, SLAVE denotes the u-blox 6 GPS receiver while MASTER denotes the external device (CPU, μC) controlling the DDC bus by driving the SCL line.

u-blox GPS receivers support Standard-Mode I²C-bus specification with 7-bit addressing and a data transfer rate up to 100 kBit/s and a SCL clock frequency up to 100 kHz.

C.1.2 DDC troubleshooting

Consider the following questions when implementing I²C in designs:

- Is there a stable supply voltage Vdd? Often, external I²C devices (like I²C masters or monitors) must be provided with Vdd.
- Are appropriate termination resistances attached between SDA, SCL and Vdd? The voltage level on SDA and SCL must be Vdd as long as the bus is idle and drop near GND if shorted to GND. [Note: Very few I²C masters exist which drive SCL high and low, i.e. the SCL line is not open-drain. In this case, a termination resistor is not needed and SCL cannot be pulled low. These masters will not work together with other masters (as they have no multi-master support) and may not be used with devices which stretch SCL during transfers.]
- Are SDA and SCL mixed up? This may accidentally happen e.g. when connecting I²C buses with cables or connectors.
- Do all I²C devices support the I²C supply voltage used on the bus?
- Do all I²C devices support the maximum SCL clock rate used on the bus?
- If more than one I²C master is connected to the bus: do all masters provide multi-master support?
- Are the high and low level voltages on SDA and SCL correct during I²C transfers? The I²C standard defines the low level threshold with 0.3 Vcc, the high level threshold with 0.7 Vcc. Modifying the termination resistance Rp, the serial resistors Rs or lowering the SCL clock rate could help here.
- Are there spikes or noise on SDA, SCL or even Vdd? They may result from interferences from other components or because the capacitances Cp and/or Cc are too high. The effects can often be reduced by using shorter interconnections.

For more information about DDC implementation refer to the u-blox 5/6 Receiver Description including Protocol Specification [2].

## C.2 SPI Interface

### C.2.1 SPI basics

Devices communicate in master/slave mode where the master device provides the clock signal (SCK) and determines the state of the chip select (SCS/SS_N) lines, i.e. it activates the slave it wants to communicate with. The slave device receives the clock and chip select from the master. Multiple slave devices are allowed with individual slave select (chip select) lines. This means that there is one master, while the number of slaves is only limited by the number of chip selects. In addition to reliability and relatively high speed (with respect to the conventional UART), the SPI interface is easy to use and requires no special handling or complex communication stack implementation in the software.

The standard configuration for a slave device (see Figure 39) uses two control and two data lines. These are identified as follows:

- **SCS** — Slave Chip Select (control: output from master, usually active low)
- **SCK** — Serial Clock (control: output from master)
- **MOSI** — Master Output, Slave Input (data: output from master)
- **MISO** — Master Input, Slave Output (data: output from slave)

Alternative naming conventions are also widely used. Confirm the pin/signal naming with specific components used.

![Figure 39: SPI slave](image)

SPI always follows the basic principle of a shift register. During an SPI transfer, command codes and data values are simultaneously transmitted (shifted out serially) and received (shifted in serially). The data is entered into a shift register and then internally available for parallel processing. The length of the shift registers is not fixed, but can vary from device to device. Normally the shift registers are 8Bit or integral multiples thereof. However, they can also have an odd number of bits. For example two cascaded 9Bit EEPROMs can store 18Bit data.

When an SPI transfer occurs, an 8-bit character is shifted out one data pin while a different 8-bit character is simultaneously shifted in a second data pin. Another way to view this transfer is that an 8-bit shift register in the master and another 8-bit shift register in the slave are connected as a circular 16-bit shift register. When a transfer occurs, this distributed shift register is shifted eight bit positions; thus, the characters in the master and slave are effectively exchanged.

The serial clock (SCK) line synchronizes shifting and sampling of the information on the two serial data lines (MOSI and MISO). The chip select (SCS/SS_N) line allows individual selection of a slave SPI device. If an SPI slave device is not selected (i.e. its chip select is not activated), its data output enters a high-impedance state (hi-Z) and does not interfere with SPI bus activities.
The data output MISO functions as the data return signal from the slave to the master.

Figure 40 shows a typical block diagram for an SPI master with several slaves. Here, the SCK and MOSI data lines are shared by all of the slaves. Also the MISO data lines are linked together and led back to the master. Only the chip selects are separately brought to each SPI device.

Figure 40: Master with independent slaves

SPI allows multiple microcontrollers to be linked together. These can be configured according to single or multiple master protocols. In the first variant the microcontroller(s) designated as slave(s) behave like a normal peripheral device. The second variant allows for several masters and allows each microprocessor the possibility to take the role of master and to address another microprocessor. In this case one microcontroller must permanently provide the clock signal.

There are two SPI system errors. The first occurs if several SPI devices want to become master at the same time. The other is a collision error that occurs for example when SPI devices work with different polarities.

Systems involving multiple microcontrollers are beyond the scope of this document.

Cascading slave peripherals is not supported.

Four I/O pin signals are associated with SPI transfers: the SCK, the MISO data line, the MOSI data line, and the active low SCS/SS_N pin. In the unselected state the MISO lines are hi-Z and therefore inactive. The master decides with which peripheral device it wants to communicate. The clock line SCK provides synchronization for data communication and is brought to the device whether or not it is selected.

The majority of SPI devices provide all four of these lines. Sometimes MOSI and MISO are multiplexed, or else one is missing. A peripheral device, which must not or cannot be configured, requires no input line but only a data output. As soon as it gets selected it starts sending data. In some ADCs therefore the MOSI line is missing. Some devices have no data output (e.g. LCD controllers which can be configured, but cannot send data or status messages).

The following rules should answer the most common questions concerning these signals:

- **SCK**: The SCK pin is an output when the SPI is configured as a master and an input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal bus clock. When the master initiates a transfer, eight clock cycles are automatically generated on the SCK pin.
When the SPI is configured as a slave, the SCK pin is an input, and the clock signal from the master synchronizes the data transfer between the master and slave devices. Slave devices ignore the SCK signal unless the slave select pin is active low. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.

- **MISO/MOSI:** The MISO and MOSI data pins are used for transmitting and receiving serial data. When the SPI is configured as a master, MISO is the master data input line, and MOSI is the master data output line. When the SPI is configured as a slave, these pins reverse roles.

- **SCS/SS_N:** In master mode, the SCS output(s) select external slaves (e.g. SCS1_N, SCS2_N). In slave mode, SS_N is the slave select input. The chip select pin behaves differently on master and slave devices. On a slave device, this pin is used to enable the SPI slave for a transfer. If the SS_N pin of a slave is inactive (high), the device ignores SCK clocks and keeps the MISO output pin in the high-impedance state. On a master device, the SCS pin can serve as a general-purpose output not affecting the SPI.
## Glossary

<table>
<thead>
<tr>
<th><strong>Abbreviation</strong></th>
<th><strong>Description</strong></th>
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<tbody>
<tr>
<td>API</td>
<td>Application Programming Interface</td>
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<tr>
<td>BBR</td>
<td>Battery backup RAM</td>
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<tr>
<td>ECEF</td>
<td>Earth Centered Earth Fixed</td>
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<tr>
<td>ESD</td>
<td>Electro Static Discharge</td>
</tr>
<tr>
<td>HAE</td>
<td>Height Above WGS84-Ellipsoid</td>
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<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
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<tr>
<td>LOS</td>
<td>Line of sight,</td>
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<tr>
<td>NMEA 0183</td>
<td>ASCII based standard data communication protocol used by GPS receivers.</td>
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<tr>
<td>PUBX</td>
<td>u-blox proprietary extension to the NMEA protocol</td>
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<tr>
<td>PVT</td>
<td>Position Velocity Time</td>
</tr>
<tr>
<td>SA</td>
<td>Selective Availability</td>
</tr>
<tr>
<td>SV</td>
<td>Satellite Vehicle</td>
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<tr>
<td>SBAS</td>
<td>Satellite Based Augmentation Systems</td>
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<tr>
<td>UBX</td>
<td>File extension for u-center log file or short form for the UBX protocol</td>
</tr>
<tr>
<td>UBX Protocol</td>
<td>A proprietary binary protocol used by the ANTARIS™ GPS technology</td>
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Related documents

[1] AMY-6M Data Sheet, Doc No GPS.G6-HW-10039
  https://webstore.iec.ch/publication/4024

Additional information is available in the FAQ section of our website (http://www.u-blox.com/en/faq.html).

For regular updates to u-blox documentation and to receive product change notifications please register on our homepage.

Revision history

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