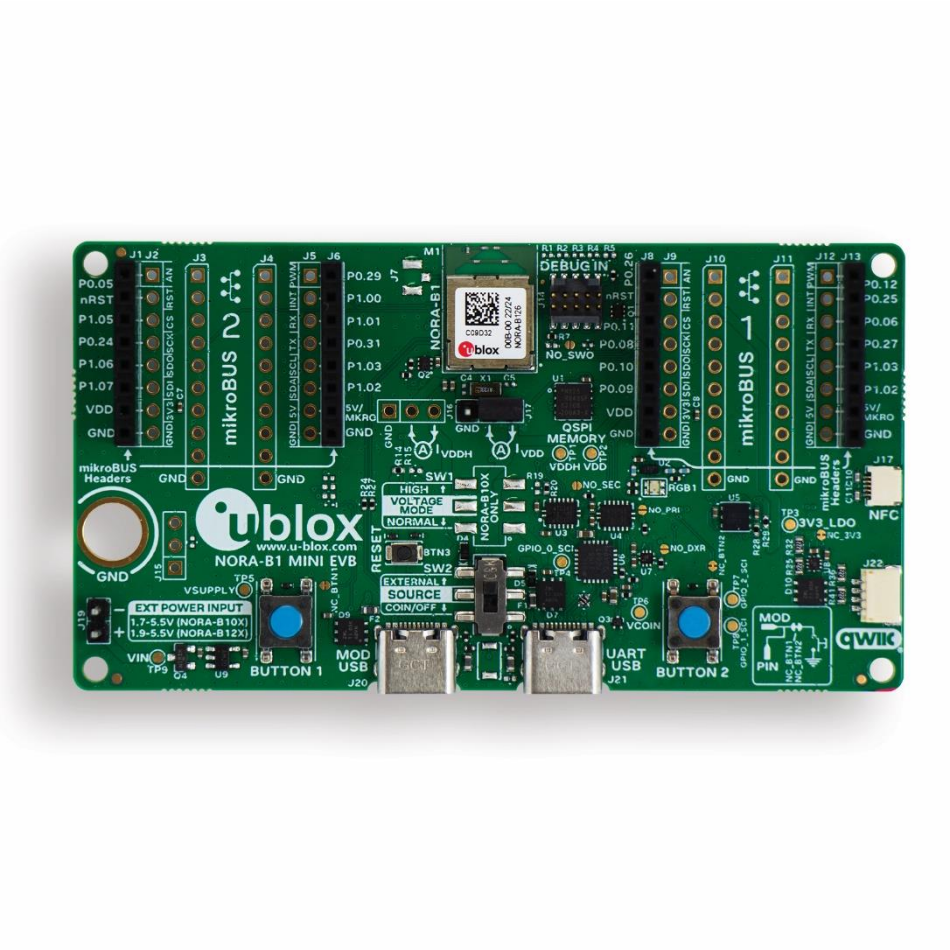
MINI-NORA-B1 EVK

Evaluation kit revision C for NORA-B1series modules

User guide



Abstract

This document describes how to set up the MINI-NORA-B1 evaluation kits to evaluate the NORA-B1 series modules. It is applicable to Rev C and newer versions of the EVK. It also describes the different options for debugging and the development capabilities included in the evaluation board.

Document information

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In development / Prototype	Objective specification	Target values. Revised and supplementary data will be published later.
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Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	**Hardware revision**	**Document status**
MINI-NORA-B106	Rev C or newer	Early production information
MINI-NORA-B126	Rev C or newer	Early production information

☞ For information about the hardware, software, and status of the available product types, see also the NORA-B1 data sheet [1].

Contents

1 Product description

The MINI-NORA-B1 evaluation kit provides stand-alone use of the NORA-B1 series module featuring the Nordic Semiconductor nRF5340 dual-core RF System on Chip (SoC).

The evaluation kit provides a great starting point for almost any Bluetooth® Low Energy (LE), Thread, or Zigbee® project. All features of the NORA-B1 series modules are easily accessed from the evaluation board. One USB connection provides power and virtual COM ports. A second USB connector also provides power and connection to the NORA-B1 USB peripheral feature. Also available are two user buttons, a user RGB LED, and a reset button. QSPI flash provides an additional 64 Mbit (8 MiB) memory, including execute-in-place (XIP). All GPIO signals of the NORA-B1 are available on headers. Two mikroBUS™ sockets allow NORA-B1 to host mikroBUS click™ and other mikroBUS add-on boards. One Qwiic® connector allows the use of external Qwiic boards. A low, 1 A, drop-out regulator (LDO) provides power to the MINI-NORA-B1. Current measurement headers allow for measuring load current used by the module.

This guide provides setup instructions for starting development and describes the hardware functionality of the MINI-NORA-B1 board, rev C and newer. For Rev B[1] hardware, see reference [17].

☞ An external debug probe or EVK-NORA-B1 is required to program and debug applications on the NORA-B1 module on MINI-NORA-B1. See Table 1.

1.1 Key features

- Evaluation platform for NORA-B106 or NORA-B126 modules
- Two virtual COM ports over USB
- Full GPIO of the NORA-B1 series
- Buttons and LED user interaction
- NFC antenna connector
- 32.768 kHz Crystal
- 64 Mbit (8 MiB) QSPI flash
- CR2032 battery holder
- USB peripheral connector
- Power input connectors
- 1A LDO regulator
- Two mikroBUS headers
- One Qwiic connector

[1] Rev A was never released to the public.

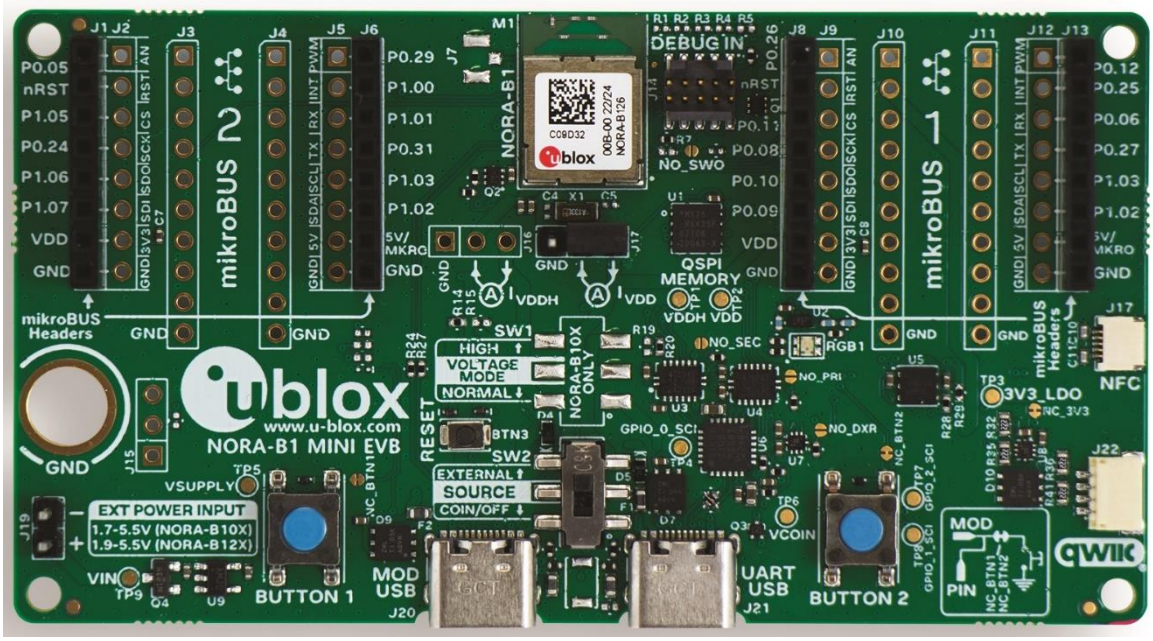

Figure 1: MINI-NORA-B1 rev C evaluation board (top view)

1.2 Kit contents

1.2.1 MINI-NORA-B106 kit contents

- MINI-NORA-B1 evaluation board with NORA-B106 module
- NFC antenna
- 2.4 GHz antenna integrated onto NORA-B106 module (no external antenna)

1.2.2 MINI-NORA-B126 kit contents

- MINI-NORA-B1 evaluation board with NORA-B126 module
- NFC antenna
- 2.4 GHz antenna integrated onto NORA-B126 module (no external antenna)

1.3 Revision identification

The revision of the EVK is shown in silkscreen on the bottom side of the PCB. See the highlighted area in Figure 2.

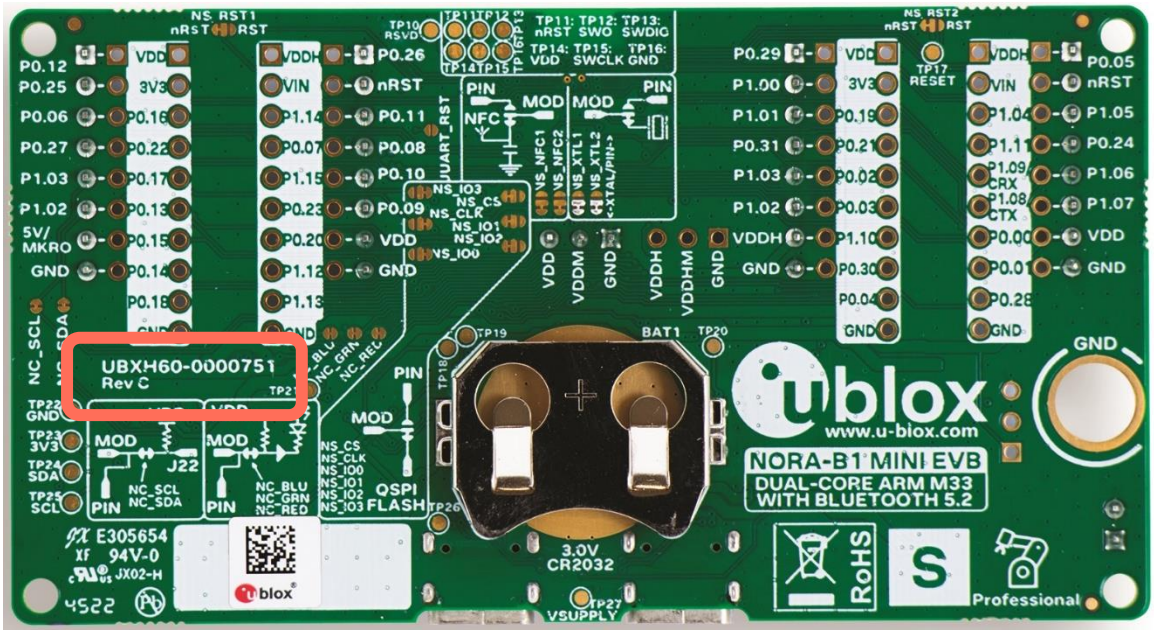

Figure 2: MINI-NORA-B1 rev C evaluation board (bottom view)

1.4 Required development tools

The tools shown in Table 1 are required for NORA-B1 series Bluetooth LE and IEEE 802.15.4 module applications.

Tool	Description
SEGGER J-Link debug probe	An external SEGGER J-Link debug probe is required to program the NORA-B1 module over the SWD port. A SEGGER J-Link or J-Trace probe [8], or EVK-NORA-B1 or Nordic Semiconductor nRF5340DK with its J-LINK-OB interface [3] may be used.
Nordic Semiconductor nRF Connect for Desktop	nRF Connect for Desktop is the primary development tool used with the NORA-B1 series modules. This tool includes an installation and maintenance utility for the nRF Connect SDK, Toolchain Manager. See also reference [11]. nRF Connect for Desktop is a cross-platform tool that also enables testing and development with Bluetooth LE. It allows easy setup of connections with other devices and uses these connections to read and write the external nodes. Available for Windows, Mac OS®, and Linux.
Nordic Semiconductor nRF Connect SDK (NCS)	nRF Connect SDK contains several components, including the Zephyr RTOS, MCUboot, and nrfxlib peripheral libraries for the nRF5340 CPU within the NORA-B1 series modules. Installation of NCS is managed through nRF Connect for Desktop. Available for 32- and 64-bit Windows, Mac OS, and 64-bit Linux platforms. See also reference [6]. Nordic Command Line Tools are installed with NCS, including nrfjprog.

Table 1: Required development tools

1.5 Optional development tools

The tools shown in Table 2 are additional, optional development tools to aid in NORA-B1 application development.

Tool	Description
Nordic Semiconductor nRF Connect for Mobile	nRF Connect for Mobile is a powerful generic tool that allows you to scan and explore your Bluetooth LE devices and communicate with them. nRF Connect for Mobile supports several Bluetooth SIG adopted profiles, as well as the Device Firmware Update profile (DFU) from Nordic Semiconductor or Eddystone from Google. Available for iOS and Android. Installation is nRF Connect for Mobile is optional. See also reference [12].
SEGGER J-Link Software and Documentation Pack	J-Link Commander (JLink.exe) is a command line-based utility that can be used for verifying proper functionality of J-Link as well as for simple analysis of the target system. It supports some simple commands, such as memory dump, halt, step, go etc. to verify the target connection. Available for Windows, Mac OS, and Linux. J-Link software may also be used in scripts for end-product programming at the factory. See also reference [9].
Nordic Semiconductor Mobile Apps	Additional, optional mobile utilities for application development. Available for iOS and Android. See also reference [13].
Nordic Semiconductor Power Profiler Kit II (PPK2)	The Power Profiler Kit II is a standalone unit, which can measure and optionally supply currents all the way from sub-mi and as high as 1A on the MINI-NORA-B1 and other hardware. See also reference [14].

Table 2: Optional development tools

2 Hardware description

Design files for the MINI-NORA-B1 PCB may be requested from the u-blox support team.

2.1 Power

The power input section of the schematic is shown in Figure 3.

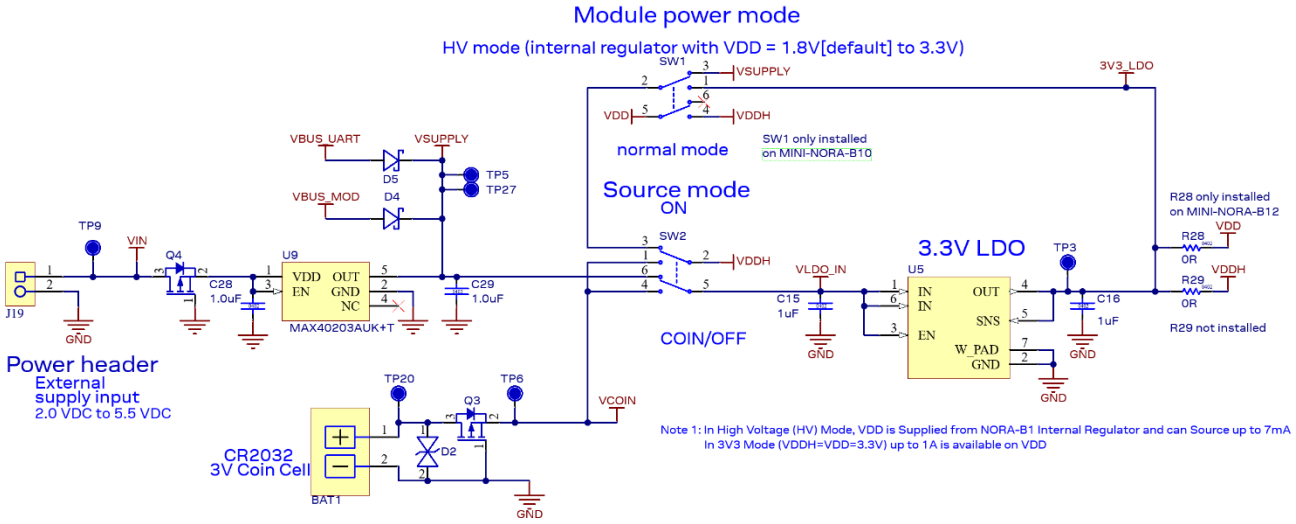

Figure 3: MINI-NORA-B1 power schematic

The MINI-NORA-B1 has four possible power sources, as described in Table 3.

Source	Voltage	Current (max.)	Remarks
USB from Virtual COM PORT (**VBUS_UART**), J21	+5 VDC nominal	500 mA	Enumerates as USB 2.0, full-speed, USB high-power
USB from NORA-B1 (**VBUS_MOD**), J20	+5 VDC nominal	100 mA	Without application code enabling USB peripheral
		500 mA	With application code enumerating as USB 2.0 peripheral in USB high-power mode
2.54 mm center pins, J19	+2.8 VDC to +5.5 VDC	1000 mA	High voltage mode (Not available for EVK-NORA-B12)
	+2.0 VDC to +5.5 VDC	1000 mA	Low voltage mode
CR2032 coin cell battery	+3 VDC nominal	-	Refer to coin cell data sheet for current capacity

Table 3: Power sources

Power settings are determined by SW1 and SW2. MINI-NORA-B10 and MINI-NORA-B12 have different component populations.

Power inputs are reverse polarity protected. This allows them to be used simultaneously with the highest voltage supply chosen.

The coin cell is isolated from the other sources to avoid the voltage drop across a protection diode. The coin cell is protected from reverse polarity.

2.1.1 MINI-NORA-B10 power settings

SW1 and SW2 are both populated on MINI-NORA-B10 to allow normal and high voltage modes of the NORA-B10 module.

Mode	Module mode SW1	Source mode SW2	Supply voltage	Remarks
OFF	Normal Down	COIN/OFF Down	Coin cell if present Board OFF if not	VDD = VDDH = V_{COIN}
Normal	Normal Down	ON Up	2.0 VDC to 5.5 VDC	GPIO voltage = VDD
Unsupported	High voltage Up	COIN/OFF Down	N/A	Running MINI-NORA-B10 in the high voltage setting from a coin cell is not recommended
High voltage	High voltage Up	ON Up	2.8 VDC to 5.5 VDC	GPIO voltage reference is set by VREGHVOUT register of the application core. Default value is 1.8 VDC.

Table 4: MINI-NORA-B10 power settings

From 2.0 VDC to 3.6 VDC input, VDD (VDDH in high voltage mode) is equal to the supply voltage minus the LDO dropout voltage (<= 265 mVDC): VDD = V_{IN} – V_{LDO}. Above 3.6 VDC input, VDD = 3.3 VDC.

Only non-rechargeable coin cells, such as the CR2032, are supported.

2.1.2 MINI-NORA-B12 power settings

Only SW2 is populated on MINI-NORA-B12. High voltage operation is not available on the NORA-B12 module.

Mode	Source mode SW2	Supply voltage	Remarks
OFF	COIN/OFF Down	OFF	Operation of MINI-NORA-B12 from a coin cell is not recommended
Normal	ON Up	2.0 VDC to 5.5 VDC	GPIO voltage = VDD

Table 5: MINI-NORA-B12 power settings

From 2.0 VDC to 3.6 VDC input, VDD=VDDH is equal to the supply voltage minus the LDO dropout voltage (<= 265 mVDC): VDD = VIN – VLDO. Above 3.6 VDC input, VDD = 3.3 VDC.

Only non-rechargeable coin cells, such as the CR2032, are supported.

2.2 Reset

The EVK primary reset circuit and button (RESET) connects to the following locations:

- NORA-B1 module **nRESET**: active low
- SWD debug connector **nRESET**: active low
- mikroBUS sockets **nRESET:** active low by default. Active high may be selected by changing **NS_RST1** and **NS_RST2** jumpers.

The Virtual COM Port (VCP) interface can also be connected to **nRESET** when the solder bridge **JUART_RST** is shorted.

2.3 Buttons

The EVK provides two active-low user buttons that connect to ground when pressed. Table 6 associates the button number and corresponding components.

Button	Switch	GPIO	Jumper
1	BTN1	P0.04	NC_BTN1
2	BTN2	P0.22	NC_BTN2

Table 6: User button components

Open the associated jumper to isolate the button from the circuit.

2.4 Tri-color LED

The EVK supports a tricolor LED – red, green, and blue (RGB). The LED is powered by **VDDH,** and each LED color can be isolated from the circuit by breaking the associated jumper. The RGB LED GPIO control signals are active low.

Color	GPIO	Jumper
Red	P0.28	NC_RED
Green	P0.30	NC_GRN
Blue	P1.11	NC_BLU

Table 7: LED signals

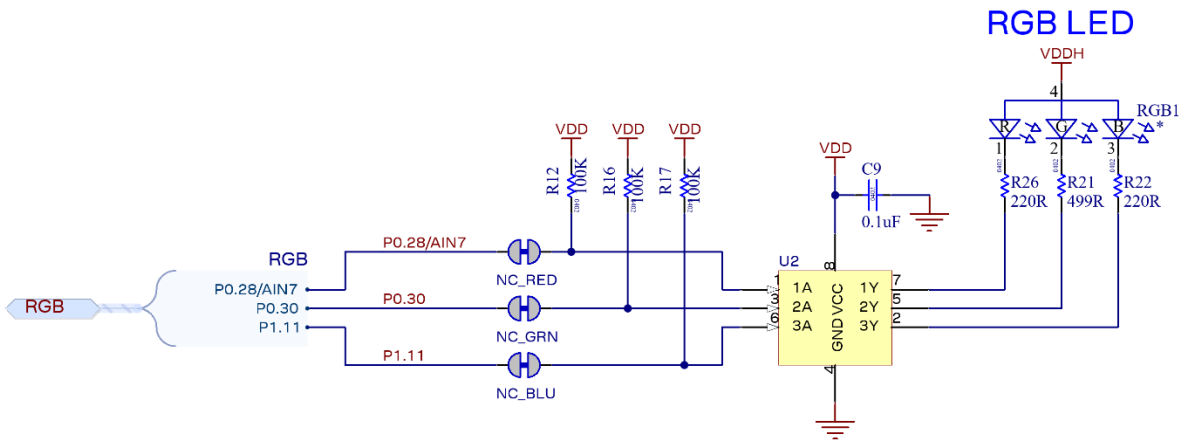

Figure 4: RGB LED schematic

The NCS board support package (BSP) for MINI-NORA-B1 configures both the Zephyr and Nordic Semiconductor LED and button service (LBS) for active-low. No modification to example source code is required.

2.5 Serial communication

The EVK provides two USB-to-serial channels – one for each processor core of the NORA-B1 module. The USB-UART interface comprises a Silicon Labs CP2105 dual UART bridge that includes an Enhanced Communications Interface (ECI) and Standard Communications Interface (SCI).

Table 8 describes the function for each UART signal.

NORA-B1 pin name	NORA-B1 function	USB serial IC function
P1.12	Application core TXD	CP2105 ECI RXD
P1.13	Application core RXD	CP2105 ECI TXD
P1.14	Application core RTS	CP2105 ECI CTS
P1.15	Application core CTS	CP2105 ECI RTS
P0.29	Standard GPIO or GPIO to USB host	CP2105 GPIO 0 ECI
P1.00	Standard GPIO or GPIO to USB host	CP2105 GPIO 1 ECI
P0.20	Network core TXD	CP2105 SCI RXD
P0.23	Network core RXD	CP2105 SCI TXD
P0.21	Network core RTS	CP2105 SCI CTS
P0.19	Network core CTS	CP2105 SCI RTS

Table 8: USB to serial/GPIO signal assignments

☞ The UART pin assignments for the NORA-B1 application and network core **TXD**, **RXD**, **RTS**, and **CTS** are different than those of the EVK-NORA-B1.

Each CP2105 UART interface includes one GPIO connected to NORA-B1. To use these signals, an application on the host PC must use the Silicon Labs device driver and DLL. Use of these signals is optional. For more information on how to configure the port pins of the CP2105, see also reference [16].

Each CP2105 UART can be isolated from NORA-B1 by shorting the associated solder jumper. Doing so frees up the associated pins in Table 8 for other assignments.

- **NO_PRI**: short to isolate the application core UART
- **NO_SEC**: short to isolate network core UART
- **NO_DXR**: short to isolate GPIO from NORA-B1

2.6 32.768 kHz low frequency clock

The low frequency (LF) clock of the NORA-B1 module is supplied from one of four possible sources:

- Internal calibrated RC oscillator (LFRC) – for applications with no strict real-time requirements
- External crystal oscillator (LFXO) – offers the most accurate and lowest power LF clock
- External source (LFXO and **OSCILLATORS.XOSC32KI.BYPASS** settings [10] – allows the use of a common clock source for other components in a system
- Synthesized LF clock (LFSYNT) derived from the system clock (HFCLK).

The EVK has a 32.768 kHz crystal connected to the NORA-B1 module to allow use of the external crystal oscillator option (LFXO), providing tighter frequency tolerances (±20 ppm). Load capacitors for the oscillator circuit are provided internal to the nRF53 integrated within the module.

To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. The load capacitance that best matches the crystal specification, 6 pF, 7 pF, or 9 pF, must then be defined in the **XOSC32KI.INTCAP** register.

The formula for calculating the required value of internal capacitor (C_{CAP}) is 2 * C_L – C_{PAD} where:

- Load capacitance (C_L) = 7 pF (crystal data sheet)
- Pad capacitance (C_{PAD}) = 4 pF (nRF53 product specification)

C_{CAP} = 2 * 7 pF – 4 pF = 10 pF. Select the closest available value for the **XOSC32KI.INTCAP** register. For this EVK, this is 9 pF.

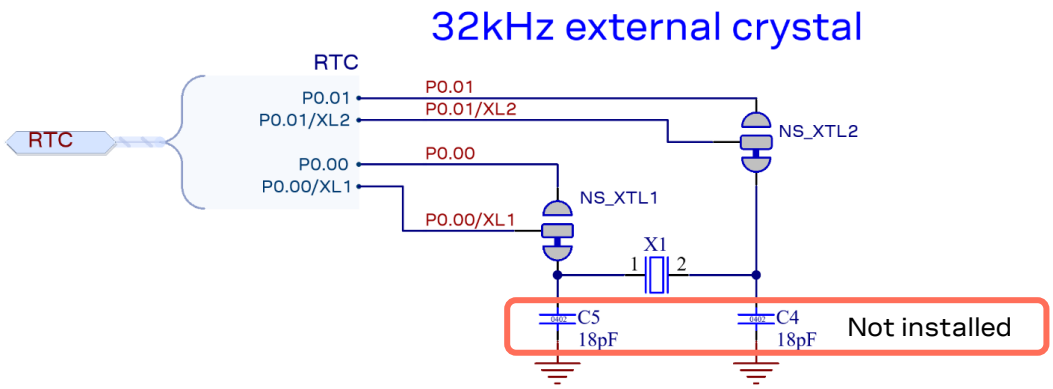

Figure 5: Schematic – 32 kHz crystal

If an internal RC oscillator or external input LF clock source is used, the crystal can be isolated from the circuit by opening jumpers **NS_XTL0** and **NS_XTL1**. Soldering across the normally open position connects **P0.00/XL1** and **P0.01/XL2** to the EVK headers.

When using an external clock source, connect it to **P0.00/XL1** and set **LFCLKSRC.SRC** to LFXO. For a low-swing source, ground P0.01 and set **OSCILLATORS.XOSC32KI.BYPASS** to disabled. For a rail-to-rail source, leave P0.01 open and set **OSCILLATORS.XOSC32KI.BYPASS** to enabled. See also reference [5].

2.7 NFC connector

Connection to an external NFC antenna is provided through a Kyocera / AVX flat-flex connector, part number 046284005001846. Capacitors C7 and C8 provide tuning of the NFC antenna for resonance at 13.56 MHz.

The values of C7 and C8 are tuned for use with the supplied NFC antenna. These values may need to be changed if a different antenna is used. See also reference [3].

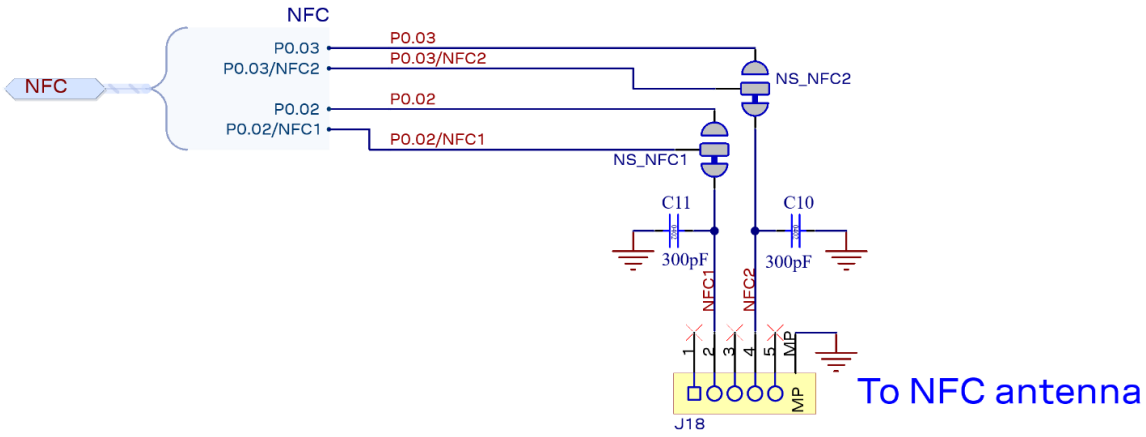

Figure 6: NFC connector

By default, the NORA-B1 module pins P0.02 and P0.03 are configured for NFC use. These pins can also be used for digital GPIO functions by modifying the position of jumpers J0.02 and J0.03 and the value of the NFCPINS UICR register of the application core.

Mode	Short position:	NS_NFC1	NS_NFC2	NS_NFC1	NS_NFC2	NFCPINS UICR register
NFC (default)				Bottom	Bottom	0xFFFFFFFF (enable protection, use as NFC)
GPIO[2,3]		Top	Top			0xFFFFFFFE (disable protection, use as GPIO)

Table 9: NFC jumper configuration

2.8 Quad SPI (QSPI) flash memory

A 64 Mbit (8 MiB) Quad SPI (MX25R6435F) flash is available on the MINI-NORA-B1. This memory can be used for execute-in- place (XIP) directly from the flash as well as for general data storage.

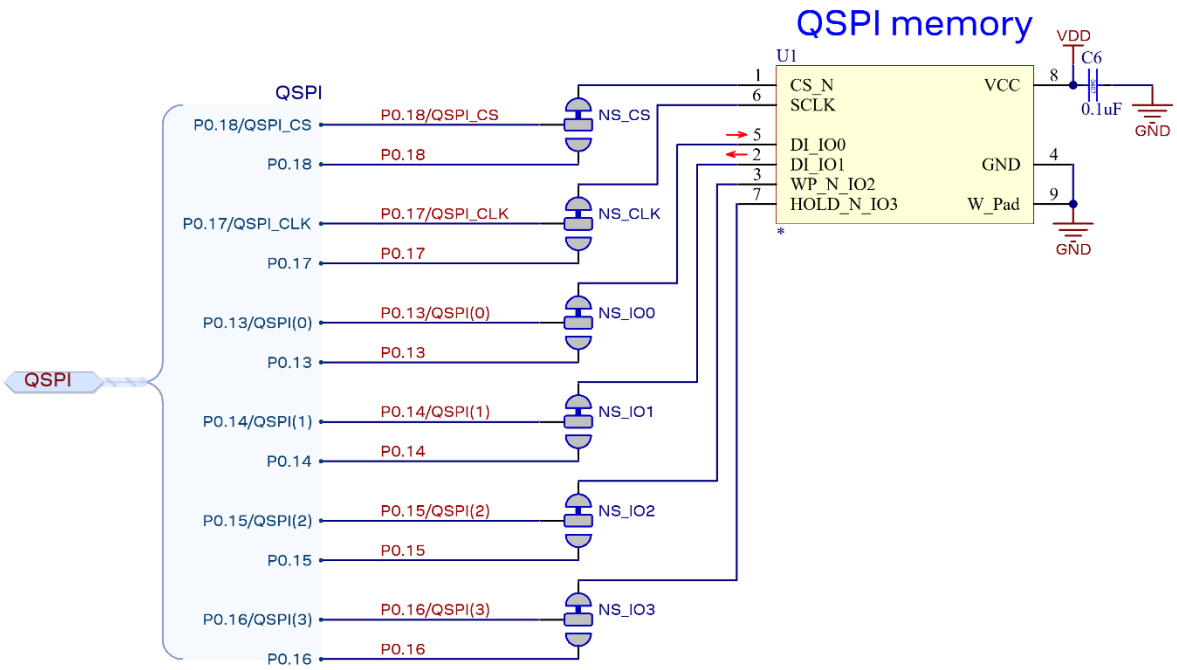

Figure 7: QSPI flash

By default, the NORA-B1 module pins P0.13 through P0.18 are configured for QSPI use. These pins can be changed to GPIO functions by modifying the position of jumpers **NS_IO0** – **NS_IO3**, **NS_CLK**, and **NS_CS**.

2.9 USB

Two USB-C connectors are provided on the MINI-NORA-B1. Either connection may be used to power the EVK.

J20 is a USB-C socket that connects to the USB peripheral of the NORA-B1 module. Application firmware must enable the USB peripheral.

⚠ Up to 500 mA may be drawn from the upstream USB host or hub when configured as a high-power, bus-powered device by the application firmware. If the firmware does not configure the USB port, a maximum of 100 mA may be drawn from the upstream port.

[2] P0.02 and P0.03 have a pad capacitance of approximately 2.5 pF higher than other GPIO pins.
[3] When used as GPIO, P0.02 and P0.03 will exhibit approximately 1 µA leakage when driven to opposite states.

J21 is a USB-C socket that connects to a dual USB-UART interface. UART port 1 is connected to the application core of the NORA-B1 module. UART port 2 is connected to the network core of the NORA-B1 module. One output and one input GPIO between the USB host ECI port and NORA-B1 are also provided.

☞ Up to 500 mA may be drawn from the upstream USB port.

2.10 SWD

Applications are loaded to both the application core and network core of the NORA-B1 module through J14, a 2x5 header on 1.27 mm centers.

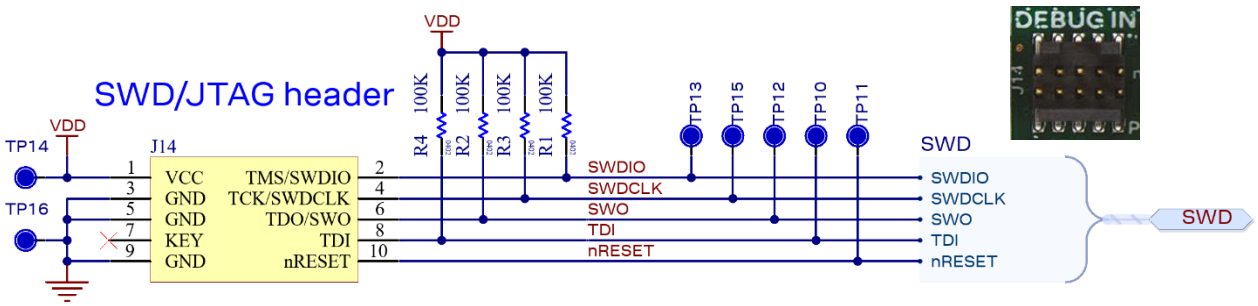

Figure 8: SWD connector

2.11 Current sensing headers

The EVK provides two current sensing headers:

- J17 allows for power consumption measurement of the NORA-B1 module VDD, MINI-NORA-B10 and MINI-NORA-B12.
- J16 allows for power consumption measurement of the NORA-B1 module VDDH, MINI-NORA-B10 only. VDDH current measurements are only valid for the high voltage setting on SW1. See Table 4.

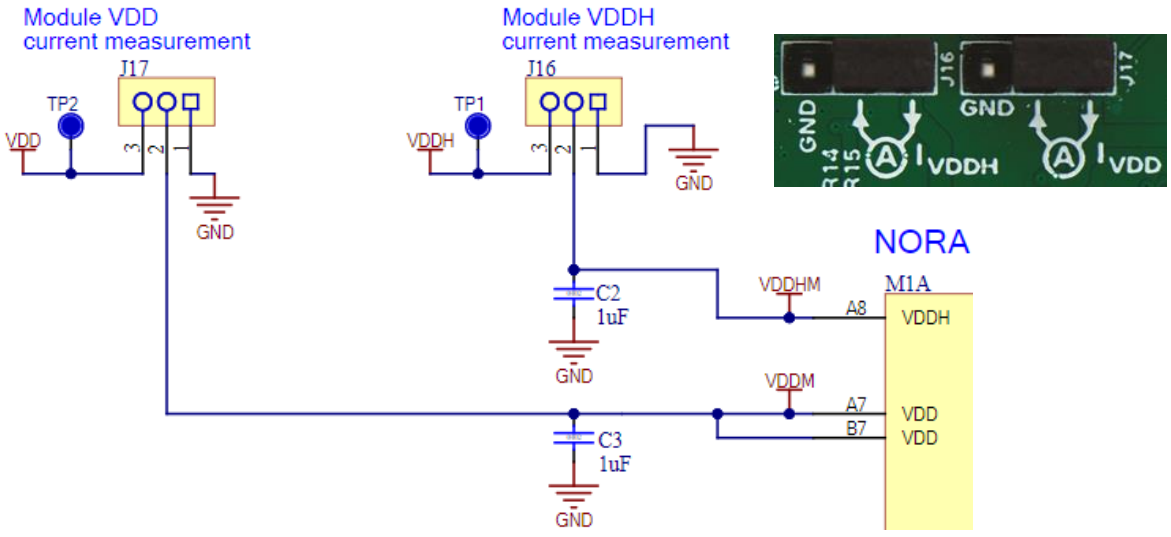

Figure 9: MINI-NORA-B10 current measurement

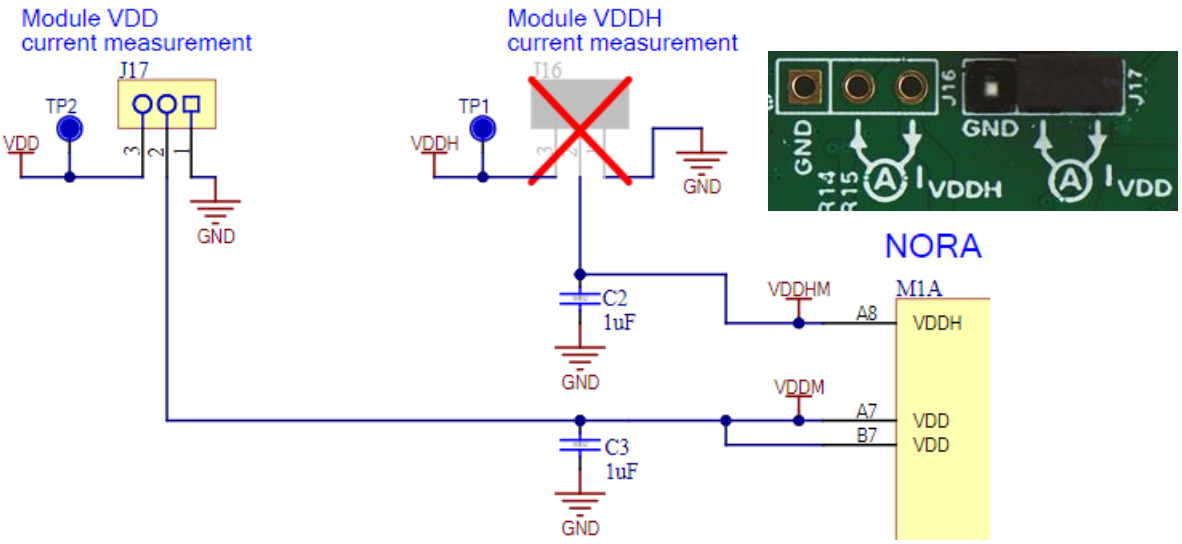

Figure 10: MINI-NORA-B12 current measurement

VDD and VDDH are connected internally on NORA-B12 modules. J16 is not installed.

2.54 mm shunts are installed from the factory across pins 2 and 3 on J16 and J17. Current can be measured by removing the shunt on each jumper. Use a current measurement device such as a DMM or power analyzer in series with pins 2 and 3 of the desired header. Current direction is shown on the PCB silkscreen.

When not measuring current, the shunts installed on pins 2 and 3 of J16 and J17 are required to ensure proper operation of the NORA-B1 module.

Pin 1 of J16 and J17 are connected to **GND**.

Only current flowing through VDD or VDDH into the module is measured; current sunk through GPIO pins is not measured.

2.12 GPIO pin assignments

Header locations on 2.54 mm centers are provided on the EVK to connect the GPIO signals.

2.12.1 mikroBUS interfaces

Two mikroBUS sockets are available to incorporate mikroBUS click and other application boards into a project. The pins are duplicated to allow connection flexibility.

A mikroBUS application board can be installed in the outer rows of pins as shown in Figure 11.

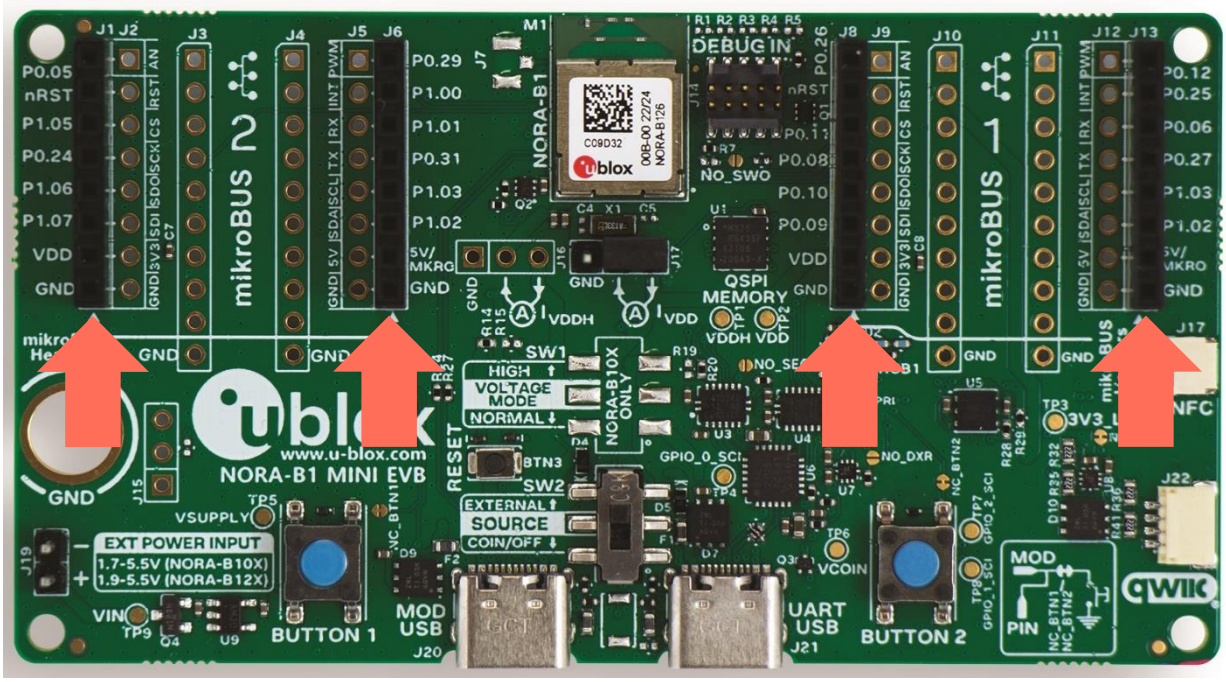

Figure 11: mikroBUS header location (header color may vary)

2.12.1.1 mikroBUS interface 1 (right)

J8 / J9 Pin	mikroBUS pin	EVK signal	Function	Remarks
1	AN	P0.26	GPIO	Analog input capable GPIO
2	nRESET (active low)	nRESET (active low)	Reset	Active high RESET is available by changing NS_RST1
3	CS	P0.11	GPIO	High-speed SPI chip select
4	SCK	P0.08	GPIO	High-speed SPI clock
5	MISO	P0.10	GPIO	High-speed SPI input
6	MOSI	P0.09	GPIO	High-speed SPI output
7	+3V3	VDD	Power	VDD depends on SW1 and SW2 positions. See also Power.
8	GND	Ground	Ground	

Table 10: mikroBUS interface 1 connector 1

J12 / J13 Pin	mikroBUS pin	EVK signal	Function	Remarks
1	PWM	P0.12	GPIO	
2	INT	P0.25	GPIO	
3	RX	P0.06	GPIO	
4	TX	P0.27	GPIO	
5	SCL	P1.03	GPIO	High-speed I2C clock[4]
6	SDA	P1.02	GPIO	High-speed I2C data[4]
7	+5V	VDDH	Power	With NORA-B126, this pin is connected to VDD. See also Power.
8	GND	GND	Ground	

Table 11: mikroBUS interface 1 connector 2

2.12.1.2 mikroBUS interface 2 (left)

J1 / J2 Pin	mikroBUS pin	EVK signal	Function	Remarks
1	AN	P0.05	GPIO	Analog input capable GPIO
2	nRESET (active low)	nRESET (active low)	Reset	Active high RESET is available by changing JRST2
3	CS	P1.05	GPIO	SPI chip select
4	SCK	P0.24	GPIO	SPI clock
5	MISO	P1.06	GPIO	SPI input
6	MOSI	P1.07	GPIO	SPI output
7	+3V3	VDD	Power	VDD depends on SW1 and SW2 positions. See also Power.
8	GND	GND	Ground	

Table 12: mikroBUS interface 2 connector 1

J5 / J6 Pin	mikroBUS pin	EVK signal	Function	Remarks
1	PWM	P0.29	GPIO	Shared with USB-UART GPIO. Short **NC_DXR** to isolate
2	INT	P1.00	GPIO	Shared with USB-UART GPIO. Short **NC_DXR** to isolate
3	RX	P1.01	GPIO	UART input
4	TX	P0.31	GPIO	UART output
5	SCL	P1.03	GPIO	High-speed I2C clock[4]
6	SDA	P1.02	GPIO	High-speed I2C data[4]
7	+5V	VDDH	Power	With NORA-B126, this pin is connected to VDD. See also Power.
8	GND	GND	Ground	

Table 13: mikroBUS interface 2 connector 2

[4] I2C is shared between both mikroBUS connectors and the Qwiic connector.

2.12.2 Qwiic interface

The I2C bus is available on a Qwiic interface for connecting other peripherals over the I2C bus.

Figure 12: Qwiic connector

J22	Qwiic pin	EVK signal	Function	Remarks
1	GND	GND	GND	
2	3.3 VDC	3V3_LDO	Power	Isolate Qwiic by cutting **NC_3V3**
3	SDA	P1.02	SDA	High-speed I2C data[5]
4	SCL	P1.03	SCL	High-speed I2C clock[5]

Table 14: Qwiic connector

The Qwiic interface can be isolated from the circuit and referenced to an external 3.3 VDC source by opening jumper **NC_3V3**.

2.12.3 Other GPIO signals

The remainder of the NORA-B1 GPIO pins are located on 10-pin headers.

J3 Pin	EVK pin name	Remarks
1	VDDH	
2	VIN	
3	P1.04	
4	P1.11	Shared with RGB LED, blue element. Cut **NC_BLU** to isolate
5	P1.09	With MINI-NORA-B12, this pin is reserved for RX_EN — FEM LNA enable
6	P1.08	With MINI-NORA-B12, this pin is reserved for TX_EN — FEM PA enable
7	P0.00	Disabled by default and shared with 32.768 KHz crystal, change **NS_XTL1** to configure for GPIO use
8	P0.01	Disabled by default and shared with 32.768 KHz crystal, change **NS_XTL2** to configure for GPIO use
9	P0.28	Shared with RGB LED, red element. Cut **NC_RED** to isolate
10	GND	

Table 15: Header J3

[5] I2C is shared between both mikroBUS connectors and the Qwiic connector.

J4 Pin	EVK pin name	Remarks
1	VDD	
2	3V3_LDO	3.3 V output of LDO
3	P0.19/SEC_NORA_CTS	Shared with USB-UART bridge, short **NO_SEC** to isolate for GPIO use
4	P0.21/SEC_NORA_RTS	Shared with USB-UART bridge, short **NO_SEC** to isolate for GPIO use
5	P0.02	Defaults to NFC antenna, change **NS_NFC1** to configure for GPIO use. See also NFC connector
6	P0.03	Defaults to NFC antenna, change **NS_NFC2** to configure for GPIO use. See also NFC connector
7	P1.10	
8	P0.30	Shared with RGB LED, green element. Cut **NC_GRN** to isolate
9	P0.04	Shared with SW1. Cut **NC_BTN1** to isolate
10	GND	

Table 16: Header J4

J10 Pin	EVK pin name	Remarks
1	VDDH	
2	VIN	
3	P1.14/PRI_NORA_RTS	Defaults to **PRI_NORA_RTS**, short **NO_PRI** to isolate for GPIO use on J10
4	P0.07	
5	P1.15/PRI_NORA_CTS	Defaults to **PRI_NORA_CTS**, short **NO_PRI** to isolate for GPIO use on J10
6	P0.23/SEC_NORA_RXD	Defaults to **PRI_NORA_RTS**, short **NO_PRI** to isolate for GPIO use on J10
7	P0.20/SEC_NORA_TXD	Defaults to **SEC_NORA_TXD**, short **NO_SEC** to isolate for GPIO use on J10
8	P1.12/PRI_NORA_TXD	Defaults to **PRI_NORA_TXD**, short **NO_PRI** to isolate for GPIO use on J10
9	P1.13/PRI_NORA_RXD	Defaults to **PRI_NORA_RXD**, short **NO_PRI** to isolate for GPIO use on J10
10	GND	

Table 17: Header J10

J11 Pin	EVK pin name	Remarks
1	VDD	
2	3V3_LDO	
3	P0.16	Disconnected by default, change **NS_IO3** to configure for GPIO use on J11
4	P0.22	Shared with BTN2, cut **NC_BTN2** to isolate for GPIO use
5	P0.17	Disconnected by default, change **NS_CLK** to configure for GPIO use on J11
6	P0.13	Disconnected by default, change **NS_IO0** to configure for GPIO use on J11
7	P0.15	Disconnected by default, change **NS_IO2** to configure for GPIO use on J11
8	P0.14	Disconnected by default, change **NS_IO1** to configure for GPIO use on J11
9	P0.18	Disconnected by default, change **NS_CS** to configure for GPIO use on J11
10	GND	

Table 18: Header J11

2.13 Antenna

The NORA-B1x6 module on the MINI-NORA-B1x6 incorporates a PCB antenna. For best performance, ensure the module antenna is not placed near metallic objects.

3 Software

3.1 Factory software

MINI-NORA-B1 is pre-loaded with the “peripheral_lbs” example provided by NCS. The advertising name is modified to “u-blox_LBS”. Instructions for testing the application are described in [18].

3.2 Development environment

Software for the MINI-NORA-B1 is developed in the same method as for the EVK-NORA-B1 and the module itself. Nordic Semiconductor nRF Connect SDK provides Zephyr RTOS, MCUboot, and nrfxlib. nRF Connect for Desktop and the Toolchain Manager provide the development environment and updates. See also references [2], [3], [6], [7], [11], and [15].

An external debug interface is required to load and debug application firmware. Suitable debug interfaces include:

- EVK-NORA-B1: a J-Link-OB interface is provided on the full EVK. The debug-out connector may be used to connect the MINI-NORA-B1 with the 10-pin cable provided with the EVK-NORA-B1. See also reference [3].
- Full J-Link debug interface: Any of the available models are suitable. See also reference [8].

3.3 Board support package

MINI-NORA-B1 requires a unique board support package (BSP) to account for the GPIO assignments within the design. An official BSP is planned for inclusion in mainline Zephyr RTOS. Until the submission is merged into the main branch, see the u-blox GitHub repository [4]. Copy the entire `ubx_mininorab10_nrf5340` and `ubx_mininorab12_nrf5340` folders into the directory `.\ncs\vX.Y.Z\zephyr\boards\arm`, where “`X.Y.Z`” is the NCS version in use.

When developing code for the application or network core of the nRF5340, select the appropriate board support package to match the module on the MINI-NORA-B1. The BSP provides the pin configurations to match the default jumper settings. Any changes to pin assignments may be accommodated through an overlay file contained within the development project, outside of the board support package folders. Further details can be found at the NCS documentation website [6].

Appendix

A Glossary

Abbreviation	Definition
ARM	Arm (Advanced RISC Machines) Holdings
CPU	Central Processing Unit
CTS	Clear To Send
DC	Direct Current
DC-DC	DC to DC converter
DFU	Device Firmware Update
EVK	Evaluation Kit
FICR	Factory Information Configuration Register
GPIO	General Purpose Input / Output
LDO	Low Drop-Out voltage regulator
LE	Low Energy
LED	Light Emitting Diode
LF	Low Frequency
LiPo	Lithium-Polymer battery
MiB	Mebibyte (2^{20} or 1048576) bytes
NCS	nRF Connect SDK
NFC	Near-Field Communications
QSPI	Quad Serial Peripheral Interface
RC	Resistor-Capacitor network
RTS	Request To Send
RXD	Receive data signal
SES	SEGGER Embedded Studio
SIG	Special Interest Group
SoC	System on Chip
SPI	Serial Peripheral Interface
TXD	Transmit data signal
UICR	User Information Configuration Register
USB	Universal Serial Bus

Table 19: Explanation of the abbreviations and terms used

Related documentation

[1] NORA-B1 data sheet, UBX-20027119
[2] NORA-B1 system integration manual, UBX-20027617
[3] EVK-NORA-B1 user guide, UBX-20030319
[4] MINI-NORA-B1 Zephyr RTOS BSP on u-blox GitHub
[5] Nordic Semiconductor nRF5340 product specification
[6] Nordic Semiconductor nRF Connect SDK documentation
[7] Nordic Semiconductor Toolchain Manager
[8] SEGGER J-Link debug probes
[9] SEGGER J-Link Software and Documentation Pack
[10] Nordic Semiconductor nRF53 LFCLK registers
[11] Nordic Semiconductor nRF Connect for Desktop
[12] Nordic Semiconductor nRF Connect for Mobile
[13] Nordic Semiconductor mobile apps
[14] Nordic Semiconductor Power Profiler Kit II
[15] Nordic Semiconductor GitHub site
[16] Silicon Labs application note AN223: Runtime GPIO Control for CP210x
[17] MINI-NORA-B1 user guide, rev B, UBX-20057806
[18] Nordic Semiconductor example, peripheral_lbs

☞ For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	02-May-2023	brec	Initial release
R02	08-Nov-2023	brec	Update document stats to early product information, updated PCBA renderings with photos of actual product.

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