TOBY-L2 and MPCI-L2 series
LTE/DC-HSPA+/EGPRS modules
System Integration Manual

Abstract
This document describes the features and the system integration of TOBY-L2 and MPCI-L2 series multi-mode cellular modules. These modules are a complete and cost efficient LTE/3G/2G solution offering up to 150 Mb/s download and 50 Mb/s upload data rates, covering up to six LTE bands, up to five WCDMA/DC-HSPA+ bands and up to four GSM/EGPRS bands in the compact TOBY LGA form factor of TOBY-L2 modules or in the industry standard PCI Express Mini Card form factor of MPCI-L2 modules.
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Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

- **AT Commands Manual**: This document provides the description of the AT commands supported by the u-blox cellular modules.
- **System Integration Manual**: This document provides the description of u-blox cellular modules’ system from the hardware and the software point of view, it provides hardware design guidelines for the optimal integration of the cellular modules in the application device and it provides information on how to set up production and final product tests on application devices integrating the cellular modules.
- **Application Note**: These documents provide guidelines and information on specific hardware and/or software topics on u-blox cellular modules. See Related documents for a list of Application Notes related to your Cellular Module.

How to use this Manual

The TOBY-L2 and MPCI-L2 series System Integration Manual provides the necessary information to successfully design and configure the u-blox cellular modules.

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:

- An index finger points out key information pertaining to module integration and performance.
- A warning symbol indicates actions that could negatively impact or damage the module.

Questions

If you have any questions about u-blox Cellular Integration:

- Read this manual carefully.
- Contact our information service on the homepage [http://www.u-blox.com/](http://www.u-blox.com/)

Technical Support

Worldwide Web

Our website ([http://www.u-blox.com/](http://www.u-blox.com/)) is a rich pool of information. Product information, technical documents can be accessed 24h a day.

By E-mail

Contact the closest Technical Support office by email. Use our service pool email addresses rather than any personal email address of our staff. This makes sure that your request is processed as soon as possible. You will find the contact details at the end of the document.

Helpful Information when Contacting Technical Support

When contacting Technical Support, have the following information ready:

- Module type (TOBY-L200) and firmware version
- Module configuration
- Clear description of your question or the problem
- A short description of the application
- Your complete contact details
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1 System description

1.1 Overview

TOBY-L2 and MPCI-L2 series comprises LTE/3G/2G multi-mode modules supporting up to six LTE bands, up to five UMTS/DC-HSPA+ bands and up to four GSM/(E)GPRS bands for voice and/or data transmission as following:

- TOBY-L200, TOBY-L201, MPCI-L200 and MPCI-L201 are designed primarily for operation in America.
- TOBY-L210 and MPCI-L210 are designed primarily for operation in Europe, Asia and other countries.
- TOBY-L220 and MPCI-L220 are designed primarily for operation in Japan.
- TOBY-L280 and MPCI-L280 are designed primarily for operation in Asia and Oceania.

TOBY-L2 and MPCI-L2 series are designed in two different form-factors suitable for applications as following:

- TOBY-L2 modules are designed in the small TOBY 152-pin Land Grid Array form-factor (35.6 x 24.8 mm), easy to integrate in compact designs and form-factor compatible with the u-blox cellular module families: this allows customers to take the maximum advantage of their hardware and software investments, and provides very short time-to-market.
  
  The modules are the perfect choice for consumer fixed-wireless terminals, mobile routers and gateways, and applications requiring video streaming. They are also optimally suited for industrial (M2M) applications, such as remote access to video cameras, digital signage, telehealth, and security and surveillance systems.

- MPCI-L2 modules are designed in the industry standard PCI Express Full-Mini Card form-factor (51 x 30 mm) easy to integrate into industrial and consumer applications and also ideal for manufacturing of small series.
  
  Typical applications are industrial computing, ruggedized terminals, video communications, wireless routers, alarm panels and surveillance, digital signage and payment systems.

With LTE Category 4 data rates at up to 150 Mb/s (down-link) and 50 Mb/s (up-link), the TOBY-L2 and MPCI-L2 series modules are ideal for applications requiring the highest data-rates and high-speed internet access.
Table 1 summarizes the TOBY-L2 and MPCI-L2 series main features and interfaces.

<table>
<thead>
<tr>
<th>Module</th>
<th>LTE</th>
<th>UMTS</th>
<th>GSM</th>
<th>Interfaces</th>
<th>Audio</th>
<th>Features</th>
<th>Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Bands</td>
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<tr>
<td>TOBY-L200</td>
<td>4</td>
<td>2,4,5</td>
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<td>7,17</td>
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<td>24</td>
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<td>850/900</td>
<td>AWS</td>
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<td>1900/2100</td>
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<tr>
<td>TOBY-L201</td>
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<td>2,4,5</td>
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<td>13,17</td>
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<td>850/1900</td>
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<td>TOBY-L210</td>
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<td>1,3,5</td>
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<td>7,8,20</td>
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<tr>
<td>TOBY-L220†</td>
<td>4</td>
<td>1,3,5</td>
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<td>8,19</td>
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<tr>
<td>TOBY-L280</td>
<td>4</td>
<td>1,3,5</td>
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<td>7,8,28</td>
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<tr>
<td>MPCI-L200</td>
<td>4</td>
<td>2,4,5</td>
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<td>7,17</td>
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<td>MPCI-L201</td>
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<td>2,4,5</td>
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<td>MPCI-L210</td>
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<td>MPCI-L220†</td>
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<td>1,3,5</td>
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<td>8,19</td>
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<tr>
<td>MPCI-L280</td>
<td>4</td>
<td>1,3,5</td>
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<td>7,8,28</td>
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</tbody>
</table>

- • = supported by all product versions
- ♦ = supported by all product versions except versions “00”, “01”
- ■ = supported by all product versions except versions “60”
- ▲ = supported by all product versions except versions “62”

Table 1: TOBY-L2 and MPCI-L2 series main features summary

TOBY-L2 modules provide Voice over LTE (VoLTE)† as well as Circuit-Switched-Fall-Back (CSFB)† audio capability.

† Not supported by “00”, “01”, “02”, “03”, “60” and “62” product versions.
† Not supported by “00”, “01”, “60”, TOBY-L201-02S and TOBY-L220-62S product versions.
Table 2 reports a summary of cellular radio access technologies characteristics and features of the modules.

<table>
<thead>
<tr>
<th>4G LTE</th>
<th>3G UMTS/HSDPA/HSUPA</th>
<th>2G GSM/GPRS/EDGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>3GPP Release 9</td>
<td>3GPP Release 8</td>
<td>3GPP Release 8</td>
</tr>
<tr>
<td>Long Term Evolution (LTE)</td>
<td>Dual-Cell HS Packet Access (DC-HSPA+)</td>
<td>Enhanced Data rate GSM Evolution (EDGE)</td>
</tr>
<tr>
<td>Frequency Division Duplex (FDD)</td>
<td>Frequency Division Duplex (FDD)</td>
<td>Time Division Multiple Access (TDMA)</td>
</tr>
<tr>
<td>DL Multi-Input Multi-Output (MIMO) 2 x 2</td>
<td>DL Rx diversity</td>
<td>DL Advanced Rx Performance (DARP) Phase 1</td>
</tr>
</tbody>
</table>

Band support¹:
- TOBY-L200 / MPCL200:
  - Band 17 (700 MHz)
  - Band 5 (850 MHz)
  - Band 4 (AWS, i.e. 1700 MHz)
  - Band 2 (1900 MHz)
  - Band 7 (2600 MHz)
- TOBY-L201 / MPCL201:
  - Band 17 (700 MHz)
  - Band 13 (750 MHz)
  - Band 5 (850 MHz)
  - Band 4 (AWS, i.e. 1700 MHz)
  - Band 2 (1900 MHz)
- TOBY-L210 / MPCL210:
  - Band 20 (800 MHz)
  - Band 5 (850 MHz)
  - Band 8 (900 MHz)
  - Band 3 (1800 MHz)
  - Band 1 (2100 MHz)
  - Band 7 (2600 MHz)
- TOBY-L220 / MPCL220:
  - Band 19 (850 MHz)
  - Band 5 (850 MHz)
  - Band 8 (900 MHz)
  - Band 3 (1800 MHz)
  - Band 1 (2100 MHz)
- TOBY-L280 / MPCL280:
  - Band 28 (750 MHz)
  - Band 5 (850 MHz)
  - Band 8 (900 MHz)
  - Band 3 (1800 MHz)
  - Band 1 (2100 MHz)
  - Band 7 (2600 MHz)

Band support²:
- TOBY-L200 / MPCL200:
  - Band 5 (850 MHz)
  - Band 8 (900 MHz)
  - Band 4 (AWS, i.e. 1700 MHz)
  - Band 2 (1900 MHz)
  - Band 1 (2100 MHz)
- TOBY-L201 / MPCL201:
  - Band 5 (850 MHz)
  - Band 2 (1900 MHz)
- TOBY-L210 / MPCL210:
  - Band 5 (850 MHz)
  - Band 8 (900 MHz)
  - Band 2 (1900 MHz)
  - Band 1 (2100 MHz)
- TOBY-L220³ / MPCL220³:
  - Band 19 (850 MHz)
  - Band 8 (900 MHz)
  - Band 1 (2100 MHz)
- TOBY-L280 / MPCL280:
  - Band 5 (850 MHz)
  - Band 8 (900 MHz)
  - Band 2 (1900 MHz)
  - Band 1 (2100 MHz)

Band support³:
- TOBY-L210 / MPCL210:
  - Band 20 (800 MHz)
  - Band 5 (850 MHz)
  - Band 8 (900 MHz)
  - Band 3 (1800 MHz)
  - Band 1 (2100 MHz)
  - Band 7 (2600 MHz)
- TOBY-L220³ / MPCL220³:
  - Band 19 (850 MHz)
  - Band 8 (900 MHz)
  - Band 1 (2100 MHz)
- TOBY-L280 / MPCL280:
  - Band 5 (850 MHz)
  - Band 8 (900 MHz)
  - Band 2 (1900 MHz)
  - Band 1 (2100 MHz)

LTE Power Class
- Class 3 (23 dBm) for LTE mode

WCDMA/HSDPA/HSUPA Power Class
- Class 3 (24 dBm) for UMTS/HSDPA/HSUPA mode

GSM/GPRS (GMSK) Power Class
- Class 4 (33 dBm) for GSM/E-GSM bands
- Class 1 (30 dBm) for DCS/PCS bands

EDGE (8-PSK) Power Class
- Class E2 (27 dBm) for GSM-E/GSM bands
- Class E2 (26 dBm) for DCS/PCS bands

Data rate
- LTE category 4: up to 150 Mb/s DL, 50 Mb/s UL

Data rate
- xxxx-L200 / xxxx-L201:
  - HSDPA cat.4, up to 21 Mb/s DL⁶
  - HSUPA cat.6, up to 5.6 Mb/s UL
- xxxx-L210 / xxxx-L220 / xxxx-L280:
  - HSDPA cat.24, up to 42 Mb/s DL
  - HSUPA cat.6, up to 5.6 Mb/s UL

Data rate⁷
- GPRS multi-slot class 12², CS1-CS4, up to 85.6 kb/s DL/UL
- EDGE multi-slot class 12², MCS1-MCS9 up to 236.8 kb/s DL/UL

Table 2: TOBY-L2 and MPCL2 series LTE, 3G and 2G characteristics summary

¹ TOBY-L2 and MPCL2 series modules support all E-UTRA channel bandwidths for each operating band according to 3GPP TS 36.521-1 [23]
³ HSDPA category 24 capable
⁴ GPRS/EDGE multi-slot class determines the number of timeslots available for upload and download and thus the speed at which data can be transmitted and received, with higher classes typically allowing faster data transfer rates.
⁵ GPRS/EDGE multi-slot class 12 implies a maximum of 4 slots in DL (reception) and 4 slots in UL (transmission) with 5 slots in total.
1.2 Architecture

Figure 1 summarizes the internal architecture of TOBY-L2 series modules.

As described in the Figure 2, each MPCI-L2 series module integrates one TOBY-L2 series module:
- The MPCI-L200 integrates a TOBY-L200 module
- The MPCI-L201 integrates a TOBY-L201 module
- The MPCI-L210 integrates a TOBY-L210 module
- The MPCI-L220 integrates a TOBY-L220 module
- The MPCI-L280 integrates a TOBY-L280 module

The TOBY-L2 module represents the core of the device, providing the related LTE/3G/2G modem and processing functionalities. Additional signal conditioning circuitry is implemented for PCI Express Mini Card compliance, and two U.F.L connectors are available for easy antenna integration.

Figure 2 shows the block diagram of the MPCI-L2 series modules.
1.2.1 Internal blocks
As described in Figure 2, each MPCI-L2 series module integrates one TOBY-L2 series module, which consists of the following internal sections: RF, baseband and power management.

RF section
The RF section is composed of RF transceiver, PAs, LNAs, crystal oscillator, filters, duplexers and RF switches.

Tx signal is pre-amplified by RF transceiver, then output to the primary antenna input/output port (ANT1) of the module via power amplifier (PA), SAW band pass filters band, specific duplexer and antenna switch.

Dual receiving paths are implemented according to LTE Down-Link MIMO 2 x 2 and 3G Receiver Diversity radio technologies supported by the modules as LTE category 4 and HSDPA category 24 User Equipments: incoming signals are received through the primary (ANT1) and the secondary (ANT2) antenna input ports which are connected to the RF transceiver via specific antenna switch, diplexer, duplexer, LNA, SAW band pass filters.

- RF transceiver performs modulation, up-conversion of the baseband I/Q signals for Tx, down-conversion and demodulation of the dual RF signals for Rx. The RF transceiver contains:
  - Automatically gain controlled direct conversion Zero-IF receiver,
  - Highly linear RF demodulator / modulator capable GMSK, 8-PSK, QPSK, 16-QAM, 64-QAM,
  - Fractional-N Sigma-Delta RF synthesizer,
  - VCO.
- Power Amplifiers (PA) amplify the Tx signal modulated by the RF transceiver
- RF switches connect primary (ANT1) and secondary (ANT2) antenna ports to the suitable Tx / Rx path
- Low Noise Amplifiers (LNA) enhance the received sensitivity
- SAW duplexers separate the Tx and Rx signal paths and provide RF filtering
- SAW band pass filters enhance the rejection of out-of-band signals
- 26 MHz crystal oscillator generates the clock reference in active-mode or connected-mode.

Baseband and power management section
The Baseband and Power Management section is composed of the following main elements:

- A mixed signal ASIC, which integrates
  - Microprocessor for control functions
  - DSP core for LTE/3G/2G Layer 1 and digital processing of Rx and Tx signal paths
  - Memory interface controller
  - Dedicated peripheral blocks for control of the USB, SIM and GPIO digital interfaces
  - Analog front end interfaces to RF transceiver ASIC
- Memory system, which includes NAND flash and LPDDR
- Voltage regulators to derive all the subsystem supply voltages from the module supply input VCC
- Voltage sources for external use: V_BCKP and V_INT (not available on MPCI-L2 series modules)
- Hardware power on
- Hardware reset
- Low power idle-mode support
- 32.768 kHz crystal oscillator to provide the clock reference in the low power idle-mode, which can be set by enable power saving configuration using the AT+UPSV command.
### 1.3 Pin-out

#### 1.3.1 TOBY-L2 series pin assignment

Table 3 lists the pin-out of the TOBY-L2 series modules, with pins grouped by function.

<table>
<thead>
<tr>
<th>Function</th>
<th>Pin Name</th>
<th>Pin No</th>
<th>I/O</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>VCC</td>
<td>70,71,72</td>
<td>I</td>
<td>Module supply input</td>
<td>VCC pins are internally connected each other. VCC supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for functional description / requirements. See section 2.2.1 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>GND</td>
<td>2, 30, 32, 44, 46, 69, 73, 74, 76, 78, 79, 80, 82, 83, 85, 86, 88-90, 92-152</td>
<td>N/A</td>
<td>Ground</td>
<td>GND pins are internally connected each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1 for functional description. See section 2.2.1 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>V_BCKP</td>
<td>3</td>
<td>I/O</td>
<td>RTC supply input/output</td>
<td>V_BCKP = 3.0 V (typical) generated by internal regulator when valid VCC supply is present. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>V_INT</td>
<td>5</td>
<td>O</td>
<td>Generic digital interfaces supply output</td>
<td>V_INT = 1.8 V (typical) generated by internal regulator when the module is switched on. Test-Point for diagnostic access is recommended. See section 1.5.3 for functional description. See section 2.2.3 for external circuit design-in.</td>
</tr>
<tr>
<td>System</td>
<td>PWR_ON</td>
<td>20</td>
<td>I</td>
<td>Power-on input</td>
<td>Internal active pull-up to the VCC enabled. See section 1.6.1 for functional description. See section 2.3.1 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>RESET_N</td>
<td>23</td>
<td>I</td>
<td>External reset input</td>
<td>Internal active pull-up to the VCC enabled. Test-Point for diagnostic access is recommended. See section 1.6.3 for functional description. See section 2.3.2 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>HOST_SELECT0</td>
<td>26</td>
<td>I</td>
<td>Selection of module configuration by the host processor</td>
<td>Not supported by all the product versions. See section 1.6.4 for functional description. See section 2.3.3 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>HOST_SELECT1</td>
<td>62</td>
<td>I</td>
<td>Selection of module configuration by the host processor</td>
<td>Not supported by all the product versions. See section 1.6.4 for functional description. See section 2.3.3 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>ANT1</td>
<td>81</td>
<td>I/O</td>
<td>Primary antenna</td>
<td>Main Tx / Rx antenna interface. 50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and application device compliance with required certification schemes. See section 1.7 for functional description / requirements. See section 2.4 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>ANT2</td>
<td>87</td>
<td>I</td>
<td>Secondary antenna</td>
<td>Rx only for MIMO 2x2 and Rx diversity. 50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and application device compliance with required certification schemes. See section 1.7 for functional description / requirements. See section 2.4 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>ANT_DET</td>
<td>75</td>
<td>I</td>
<td>Antenna detection</td>
<td>Not supported by “00”, “01”, “60” product versions. See section 1.7.2 for functional description. See section 2.4.2 for external circuit design-in.</td>
</tr>
<tr>
<td>Function</td>
<td>Pin Name</td>
<td>Pin No</td>
<td>I/O</td>
<td>Description</td>
<td>Remarks</td>
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<td>------------------------------------------------------------------------------</td>
<td>---------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>SIM</td>
<td>VSIM</td>
<td>59</td>
<td>O</td>
<td>SIM supply output</td>
<td>VSIM = 1.8 V / 3 V output as per the connected SIM type. See section 1.8 for functional description. See section 2.5 for external circuit design-in.</td>
</tr>
<tr>
<td>SIM_IO</td>
<td></td>
<td>57</td>
<td>I/O</td>
<td>SIM data</td>
<td>Data input/output for 1.8 V / 3 V SIM Internal 4.7 kΩ pull-up to VSIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.</td>
</tr>
<tr>
<td>SIM_CLK</td>
<td></td>
<td>56</td>
<td>O</td>
<td>SIM clock</td>
<td>3.43 MHz clock output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.</td>
</tr>
<tr>
<td>SIM_RST</td>
<td></td>
<td>58</td>
<td>O</td>
<td>SIM reset</td>
<td>Reset output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.</td>
</tr>
<tr>
<td>USB</td>
<td>VUSB_DET</td>
<td>4</td>
<td>I</td>
<td>USB detect input</td>
<td>Leave unconnected: VUSB_DET functionality is not supported. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.</td>
</tr>
<tr>
<td>USB_D-</td>
<td></td>
<td>27</td>
<td>I/O</td>
<td>Data Line D-</td>
<td>USB interface for AT commands, data communication, FOAT, FW update by u-blox EasyFlash tool and diagnostic. 90 Ω nominal differential impedance (Zo) 30 Ω nominal common mode impedance (Zcm) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [7] are part of the USB pad driver and need not be provided externally. If the USB interface is not used by the Application Processor, Test-Point for diagnostic / FW update access is recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.</td>
</tr>
<tr>
<td>USB_D+</td>
<td></td>
<td>28</td>
<td>I/O</td>
<td>Data Line D+</td>
<td>USB interface for AT commands, data communication, FOAT, FW update by u-blox EasyFlash tool and diagnostic. 90 Ω nominal differential impedance (Zo) 30 Ω nominal common mode impedance (Zcm) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [7] are part of the USB pad driver and need not be provided externally. If the USB interface is not used by the Application Processor, Test-Point for diagnostic / FW update access is recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.</td>
</tr>
<tr>
<td>Function</td>
<td>Pin Name</td>
<td>Pin No</td>
<td>I/O</td>
<td>Description</td>
<td>Remarks</td>
</tr>
<tr>
<td>----------</td>
<td>----------</td>
<td>--------</td>
<td>-----</td>
<td>-------------------------</td>
<td>-------------------------------------------------------------------------</td>
</tr>
<tr>
<td>UART</td>
<td>RXD</td>
<td>17</td>
<td>O</td>
<td>UART data output</td>
<td>Not supported by &quot;00&quot; product versions. 1.8 V output, Circuit 104 (RXD) in ITU-T V.24, for AT command, data communication, FOAT, diagnostic. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.</td>
</tr>
<tr>
<td>TXD</td>
<td>16</td>
<td>I</td>
<td></td>
<td>UART data input</td>
<td></td>
</tr>
<tr>
<td>CTS</td>
<td>15</td>
<td>O</td>
<td></td>
<td>UART clear to send output</td>
<td>Not supported by &quot;00&quot; product versions. 1.8 V output, Circuit 106 (CTS) in ITU-T V.24. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.</td>
</tr>
<tr>
<td>RTS</td>
<td>14</td>
<td>I</td>
<td></td>
<td>UART ready to send input</td>
<td>Not supported by &quot;00&quot; product versions. 1.8 V output, Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to V_INT. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.</td>
</tr>
<tr>
<td>DSR</td>
<td>10</td>
<td>O / I/O</td>
<td></td>
<td>UART data set ready output / GPIO</td>
<td>UART DSR not supported by &quot;00&quot; product versions; GPIO not supported by &quot;00&quot;, &quot;01&quot;, &quot;60&quot; versions. 1.8 V, Circuit 107 in ITU-T V.24, configurable as GPIO. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.2 and 1.11 for functional description. See section 2.6.2 and 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td>RI</td>
<td>11</td>
<td>O / I/O</td>
<td></td>
<td>UART ring indicator output / GPIO</td>
<td>Rl not supported by &quot;00&quot; product versions; GPIO not supported by &quot;00&quot;, &quot;01&quot;, &quot;60&quot; versions. 1.8 V, Circuit 125 in ITU-T V.24, configurable as GPIO. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.2 and 1.11 for functional description. See section 2.6.2 and 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td>DTR</td>
<td>13</td>
<td>I / I/O</td>
<td></td>
<td>UART data terminal ready input / GPIO</td>
<td>UART DTR not supported by &quot;00&quot; product versions; GPIO not supported by &quot;00&quot;, &quot;01&quot;, &quot;60&quot; versions. 1.8 V, Circuit 108/2 in ITU-T V.24, configurable as GPIO. Internal active pull-up to V_INT when configured as DTR. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.2 and 1.11 for functional description. See section 2.6.2 and 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td>DCD</td>
<td>12</td>
<td>O / I/O</td>
<td></td>
<td>UART data carrier detect output / GPIO</td>
<td>UART DCD not supported by &quot;00&quot; product versions; GPIO not supported by &quot;00&quot;, &quot;01&quot;, &quot;60&quot; versions. 1.8 V, Circuit 109 in ITU-T V.24, configurable as GPIO. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.2 and 1.11 for functional description. See section 2.6.2 and 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td>Function</td>
<td>Pin Name</td>
<td>Pin No</td>
<td>I/O</td>
<td>Description</td>
<td>Remarks</td>
</tr>
<tr>
<td>----------</td>
<td>----------</td>
<td>--------</td>
<td>-----</td>
<td>-------------</td>
<td>---------</td>
</tr>
<tr>
<td>DDC</td>
<td>SCL</td>
<td>54</td>
<td>O</td>
<td>i'C bus clock line</td>
<td>Not supported by versions '00', '01', '60', TOBY-L201-02S. 1.8 V open drain, for communication with I2C-slave devices. External pull-up required. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>SDA</td>
<td>55</td>
<td>I/O</td>
<td>i'C bus data line</td>
<td>Not supported by versions '00', '01', '60', TOBY-L201-02S. 1.8 V open drain, for communication with I2C-slave devices. External pull-up required. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.</td>
</tr>
<tr>
<td>SDIO</td>
<td>SDIO_D0</td>
<td>66</td>
<td>I/O</td>
<td>SDIO serial data [0]</td>
<td>Not supported by &quot;00&quot;, &quot;01&quot;, &quot;60&quot; product versions. SDIO interface for communication with u-blox Wi-Fi module See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>SDIO_D1</td>
<td>68</td>
<td>I/O</td>
<td>SDIO serial data [1]</td>
<td>Not supported by &quot;00&quot;, &quot;01&quot;, &quot;60&quot; product versions. SDIO interface for communication with u-blox Wi-Fi module See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>SDIO_D2</td>
<td>63</td>
<td>I/O</td>
<td>SDIO serial data [2]</td>
<td>Not supported by &quot;00&quot;, &quot;01&quot;, &quot;60&quot; product versions. SDIO interface for communication with u-blox Wi-Fi module See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>SDIO_D3</td>
<td>67</td>
<td>I/O</td>
<td>SDIO serial data [3]</td>
<td>Not supported by &quot;00&quot;, &quot;01&quot;, &quot;60&quot; product versions. SDIO interface for communication with u-blox Wi-Fi module See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>SDIO_CLK</td>
<td>64</td>
<td>O</td>
<td>SDIO serial clock</td>
<td>Not supported by &quot;00&quot;, &quot;01&quot;, &quot;60&quot; product versions. SDIO interface for communication with u-blox Wi-Fi module See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>SDIO_CMD</td>
<td>65</td>
<td>I/O</td>
<td>SDIO command</td>
<td>Not supported by &quot;00&quot;, &quot;01&quot;, &quot;60&quot; product versions. SDIO interface for communication with u-blox Wi-Fi module See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.</td>
</tr>
<tr>
<td>Audio</td>
<td>I2S_TXD</td>
<td>51</td>
<td>O / I/O</td>
<td>i'S transmit data / GPIO</td>
<td>i'S not supported by vers. '00', '01', '60', 'L201-02', 'L220-62' GPIO not supported by versions '00', '01', '60'. i'S transmit data output, alternatively configurable as GPIO. See sections 1.10 and 1.11 for functional description. See sections 2.7 and 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>I2S_RXD</td>
<td>53</td>
<td>I / I/O</td>
<td>i'S receive data / GPIO</td>
<td>i'S not supported by vers. '00', '01', '60', 'L201-02', 'L220-62' GPIO not supported by versions '00', '01', '60'. i'S receive data input, alternatively configurable as GPIO. See sections 1.10 and 1.11 for functional description. See sections 2.7 and 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>I2S_CLK</td>
<td>52</td>
<td>I/O / I/O</td>
<td>i'S clock / GPIO</td>
<td>i'S not supported by vers. '00', '01', '60', 'L201-02', 'L220-62' GPIO not supported by versions '00', '01', '60'. i'S serial clock, alternatively configurable as GPIO. See sections 1.10 and 1.11 for functional description. See sections 2.7 and 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>I2S_WA</td>
<td>50</td>
<td>I/O / I/O</td>
<td>i'S word alignment / GPIO</td>
<td>i'S not supported by vers. '00', '01', '60', 'L201-02', 'L220-62' GPIO not supported by versions '00', '01', '60'. i'S word alignment, alternatively configurable as GPIO. See sections 1.10 and 1.11 for functional description. See sections 2.7 and 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td>Function</td>
<td>Pin Name</td>
<td>Pin No</td>
<td>I/O</td>
<td>Description</td>
<td>Remarks</td>
</tr>
<tr>
<td>----------</td>
<td>----------</td>
<td>--------</td>
<td>-----</td>
<td>-------------</td>
<td>---------</td>
</tr>
<tr>
<td>GPIO</td>
<td>GPIO1</td>
<td>21</td>
<td>I/O</td>
<td>GPIO</td>
<td>Not supported by “00”, “01”, “60” product versions, providing WWAN status indication on GPIO1 pin. 1.8 V GPIO with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td>GPIO2</td>
<td>22</td>
<td></td>
<td>I/O</td>
<td>GPIO</td>
<td>Not supported by “00”, “01”, “60” product versions. 1.8 V GPIO with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td>GPIO3</td>
<td>24</td>
<td></td>
<td>I/O</td>
<td>GPIO</td>
<td>Not supported by “00”, “01”, “60” product versions. 1.8 V GPIO with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td>GPIO4</td>
<td>25</td>
<td></td>
<td>I/O</td>
<td>GPIO</td>
<td>Not supported by “00”, “01”, “60” product versions. 1.8 V GPIO with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td>GPIO5</td>
<td>60</td>
<td></td>
<td>I/O</td>
<td>GPIO</td>
<td>Not supported by “00”, “01”, “60” product versions. 1.8 V GPIO with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td>GPIO6</td>
<td>61</td>
<td></td>
<td>I/O</td>
<td>GPIO</td>
<td>Not supported by “00”, “01”, “60” product versions. 1.8 V GPIO with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.</td>
</tr>
<tr>
<td>Reserved</td>
<td>RSVD</td>
<td>6</td>
<td>N/A</td>
<td>Reserved pin</td>
<td>This pin must be connected to ground. See section 2.10</td>
</tr>
<tr>
<td>RSVD</td>
<td>1, 7-9, 18, 19, 29, 31, 33-43, 45, 47-49, 77, 84, 91</td>
<td>N/A</td>
<td>Reserved pin</td>
<td>Leave unconnected. See section 2.10</td>
<td></td>
</tr>
</tbody>
</table>

Table 3: TOBY-L2 series module pin definition, grouped by function
## 1.3.2 MPCI-L2 series pin assignment

Table 4 lists the pin-out of the MPCI-L2 series modules, with pins grouped by function.

<table>
<thead>
<tr>
<th>Function</th>
<th>Pin Name</th>
<th>Pin No</th>
<th>I/O</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power</strong></td>
<td>3.3Vaux</td>
<td>2, 24, 39, 41, 42, 52</td>
<td>I</td>
<td>Module supply input</td>
<td>3.3Vaux pins are internally connected each other. 3.3Vaux supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for functional description and requirements for the 3.3Vaux module supply. See section 2.2.1 for external circuit design-in.</td>
</tr>
<tr>
<td><strong>GND</strong></td>
<td></td>
<td>4, 9, 15, 18, 21, 26, 27, 29, 34, 35, 37, 40, 43, 50</td>
<td>N/A</td>
<td>Ground</td>
<td>GND pins are internally connected each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1 for functional description. See section 2.2.1 for external circuit design-in.</td>
</tr>
<tr>
<td><strong>Auxiliary Signals</strong></td>
<td>PERST#</td>
<td>22</td>
<td>I</td>
<td>External reset input</td>
<td>Internal 45 kΩ pull-up to 3.3 V supply. See section 1.6.3 for functional description. See section 2.3.2 for external circuit design-in.</td>
</tr>
<tr>
<td><strong>Antennas</strong></td>
<td>ANT1</td>
<td>U.FL</td>
<td>I/O</td>
<td>Primary antenna</td>
<td>Main Tx / Rx antenna interface. 50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.7 for functional description / requirements. See section 2.4 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>ANT2</td>
<td>U.FL</td>
<td>I</td>
<td>Secondary antenna</td>
<td>Rx only for MIMO 2x2 and Rx diversity. 50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.7 for functional description / requirements. See section 2.4 for external circuit design-in.</td>
</tr>
<tr>
<td><strong>SIM</strong></td>
<td>UIM_PWR</td>
<td>8</td>
<td>O</td>
<td>SIM supply output</td>
<td>UIM_PWR = 1.8 V / 3 V automatically generated according to the connected SIM type. See section 1.8 for functional description. See section 2.5 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>UIM_DATA</td>
<td>10</td>
<td>VO</td>
<td>SIM data</td>
<td>Data input/output for 1.8 V / 3 V SIM Internal 4.7 kΩ pull-up to UIM_PWR. See section 1.8 for functional description. See section 2.5 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>UIM_CLK</td>
<td>12</td>
<td>O</td>
<td>SIM clock</td>
<td>3.43 MHz clock output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>UIM_RESET</td>
<td>14</td>
<td>O</td>
<td>SIM reset</td>
<td>Reset output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.</td>
</tr>
<tr>
<td>Function</td>
<td>Pin Name</td>
<td>Pin No</td>
<td>I/O</td>
<td>Description</td>
<td>Remarks</td>
</tr>
<tr>
<td>----------</td>
<td>----------</td>
<td>--------</td>
<td>-----</td>
<td>-------------</td>
<td>---------</td>
</tr>
<tr>
<td>USB</td>
<td>USB_D-</td>
<td>36</td>
<td>I/O</td>
<td>USB Data Line D-</td>
<td>USB interface for AT commands, data communication, FOAT, FW update by u-blox EasyFlash tool and diagnostic. 90 Ω nominal differential impedance ($Z_d$) 30 Ω nominal common mode impedance ($Z_{cm}$) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [7] are part of the USB pad driver and need not be provided externally. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>USB_D+</td>
<td>38</td>
<td>I/O</td>
<td>USB Data Line D+</td>
<td>USB interface for AT commands, data communication, FOAT, FW update by u-blox EasyFlash tool and diagnostic. 90 Ω nominal differential impedance ($Z_d$) 30 Ω nominal common mode impedance ($Z_{cm}$) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [7] are part of the USB pad driver and need not be provided externally. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.</td>
</tr>
<tr>
<td>Specific Signals</td>
<td>LED_WWAN#</td>
<td>42</td>
<td>O</td>
<td>LED indicator output</td>
<td>Open drain active low output. See section 1.12 for functional description. See section 2.9 for external circuit design-in.</td>
</tr>
<tr>
<td></td>
<td>W_DISABLE#</td>
<td>20</td>
<td>I</td>
<td>Wireless radio disable input</td>
<td>Internal 22 kΩ pull-up to 3.3Vaux. See section 1.12 for functional description. See section 2.9 for external circuit design-in.</td>
</tr>
<tr>
<td>Not Connected</td>
<td>NC</td>
<td>1, 3, 5-7, 11, 13, 16, 17, 19, 23, 25, 28, 30-33, 44-46, 47-49, 51</td>
<td>N/A</td>
<td>Not connected</td>
<td>Internally not connected. See section 1.14 for the description.</td>
</tr>
</tbody>
</table>

Table 4: MPCI-L2 series module pin definition, grouped by function
1.4 Operating modes

TOBY-L2 and MPCI-L2 series modules have several operating modes. The operating modes are defined in Table 5 and described in detail in Table 6, providing general guidelines for operation.

<table>
<thead>
<tr>
<th>General Status</th>
<th>Operating Mode</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-down</td>
<td>Not-Powered Mode</td>
<td>VCC or 3.3Vaux supply not present or below operating range: module is switched off.</td>
</tr>
<tr>
<td></td>
<td>Power-Off Mode</td>
<td>VCC or 3.3Vaux supply within operating range and module is switched off.</td>
</tr>
<tr>
<td>Normal Operation</td>
<td>Idle-Mode</td>
<td>Module processor core runs with 32 kHz reference generated by the internal oscillator.</td>
</tr>
<tr>
<td></td>
<td>Active-Mode</td>
<td>Module processor core runs with 26 MHz reference generated by the internal oscillator.</td>
</tr>
<tr>
<td></td>
<td>Connected-Mode</td>
<td>RF Tx/Rx data connection enabled and processor core runs with 26 MHz reference.</td>
</tr>
</tbody>
</table>

Table 5: TOBY-L2 and MPCI-L2 series modules operating modes definition

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>Description</th>
<th>Transition between operating modes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Not-Powered Mode</td>
<td>Module is switched off. Application interfaces are not accessible.</td>
<td>When VCC or 3.3Vaux supply is removed, the modules enter not-powered mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>When in not-powered mode, TOBY-L2 modules cannot be switched on by PWR_ON, RESET_N or RTC alarm and enter active-mode after applying VCC supply (see 1.6.1).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>When in not-powered mode, MPCI-L2 modules cannot be switched on by RTC alarm and enter active-mode after applying 3.3Vaux supply (see 1.6.1).</td>
</tr>
<tr>
<td>Power-Off Mode</td>
<td>Module is switched off: normal shutdown by an appropriate power-off event (see 1.6.2). Application interfaces are not accessible. MPCL-L2 modules do not support Power-Off Mode but halt mode (see 1.6.2 and u-blox AT Commands Manual [3], AT+CFUN=127 command).</td>
<td>When the modules are switched off by an appropriate power-off event (see 1.6.2), the modules enter power-off mode from active-mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>When in power-off mode, TOBY-L2 modules can be switched on by PWR_ON, RESET_N or an RTC alarm. When in power-off mode, TOBY-L2 modules enter the not-powered mode after removing VCC supply.</td>
</tr>
</tbody>
</table>
| Idle-Mode               | Module is switched on with application interfaces temporarily disabled or suspended: the module is temporarily not ready to communicate with an external device by means of the application interfaces as configured to reduce the current consumption. The module enters the low power idle-mode whenever possible if power saving is enabled by AT+UPSV (see u-blox AT Commands Manual [3]) reducing current consumption (see 1.5.1.5). With HW flow control enabled and AT+UPSV=1 or AT+UPSV=3, the UART CTS line indicates when the UART is enabled (see 1.9.2.3, 1.9.2.4). With HW flow control disabled, the UART CTS line is fixed to ON state (see 1.9.2.3). Power saving configuration is not enabled by default: it can be enabled by the AT+UPSV command (see the u-blox AT Commands Manual [3]). | The modules automatically switch from active-mode to low power idle-mode whenever possible if power saving is enabled (see sections 1.5.1.5, 1.9.1.4, 1.9.2.4 and u-blox AT Commands Manual [3], AT+UPSV). The modules wake up from low power idle-mode to active-mode in the following events:  
  - Automatic periodic monitoring of the paging channel for the paging block reception according to network conditions (see 1.5.1.5)  
  - The connected USB host forces a remote wakeup of the module as USB device (see 1.9.1.4)  
  - Automatic periodic enable of the UART interface to receive / send data, with AT+UPSV=1 (see 1.9.2.4)  
  - Data received over UART, with HW flow control disabled and power saving enabled (see 1.9.2.4)  
  - RTS input set ON by the host DTE, with HW flow control disabled and AT+UPSV=2 (see 1.9.2.4)  
  - DTR input set ON by the host DTE, with AT+UPSV=3 (see 1.9.2.4)  
  - The connected SDO interface forces a wakeup of the module as SDO host (see 1.9.4)  
  - A preset RTC alarm occurs (see u-blox AT Commands Manual [3], AT+CALA) |
Operating Mode | Description | Transition between operating modes
---|---|---
**Active-Mode** | Module is switched on with application interfaces enabled or not suspended: the module is ready to communicate with an external device by means of the application interfaces unless power saving configuration is enabled by AT+UPSV (see sections 1.9.1.4, 1.9.2.4 and u-blox AT Commands Manual [3]). | When the modules are switched on by an appropriate power-on event (see 1.6.1), the module enters active-mode from power-off mode. If power saving configuration is enabled by the AT+UPSV command, the module automatically switches from active to idle-mode whenever possible and the module wakes up from idle to active-mode in the events listed above (see idle-mode to active-mode transition description above). When a RF Tx/Rx data connection is initiated or when RF Tx/Rx is required due to a connection previously initiated, the module switches from active to connected-mode. |

**Connected-Mode** | RF Tx/Rx data connection is in progress. The module is prepared to accept data signals from an external device unless power saving configuration is enabled by AT+UPSV (see sections 1.9.1.4, 1.9.2.4 and u-blox AT Commands Manual [3]). | When a data connection is initiated, the module enters connected-mode from active-mode. Connected-mode is suspended if Tx/Rx data is not in progress, due to connected discontinuous reception and fast dormancy capabilities of the module and according to network environment settings and scenario. In such case, the module automatically switches from connected to active mode and then, if power saving configuration is enabled by the AT+UPSV command, the module automatically switches to idle-mode whenever possible. Vice-versa, the module wakes up from idle to active mode and then connected mode if RF Tx/Rx is necessary. When a data connection is terminated, the module returns to the active-mode. |

**Table 6: TOBY-L2 and MPCI-L2 series modules operating modes description**

Figure 3 describes the transition between the different operating modes.

---

![Figure 3: TOBY-L2 and MPCI-L2 series modules operating modes transition](image-url)
1.5 Supply interfaces

1.5.1 Module supply input (VCC or 3.3Vaux)

TOBY-L2 modules are supplied via the three VCC pins, and MPCI-L2 modules are supplied via the five 3.3Vaux pins. All supply voltages used inside the modules are generated from the VCC or the 3.3Vaux supply input by integrated voltage regulators, including the V_BCKP RTC supply, the V_INT generic digital interface supply, and the VSIM or UIIM_PWR SIM interface supply.

The current drawn by the TOBY-L2 and MPCI-L2 series modules through the VCC or 3.3Vaux pins can vary by several orders of magnitude depending on radio access technology, operation mode and state. It is important that the supply source is able to support both the high peak of current consumption during 2G transmission at maximum RF power level (as described in the section 1.5.1.2) and the high average current consumption during 3G and LTE transmission at maximum RF power level (as described in the sections 1.5.1.3 and 1.5.1.4).

1.5.1.1 VCC or 3.3Vaux supply requirements

Table 7 summarizes the requirements for the VCC or 3.3Vaux modules supply. See section 2.2.1 for suggestions to properly design a VCC or 3.3Vaux supply circuit compliant with the requirements listed in Table 7.

The supply circuit affects the RF compliance of the device integrating TOBY-L2 and MPCI-L2 series modules with applicable required certification schemes as well as antenna circuit design. Compliance is guaranteed if the requirements summarized in the Table 7 are fulfilled.

<table>
<thead>
<tr>
<th>Item</th>
<th>Requirement</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC or 3.3Vaux nominal voltage</td>
<td>Within VCC or 3.3Vaux normal operating range: See &quot;Supply/Power pins&quot; section in the TOBY-L2 Data Sheet [1] or in the MPCI-L2 Data Sheet [2].</td>
<td>The modules cannot be switched on if the supply voltage is below the normal operating range minimum limit.</td>
</tr>
<tr>
<td>VCC or 3.3Vaux voltage during normal operation</td>
<td>Within VCC or 3.3Vaux extended operating range: See &quot;Supply/Power pins&quot; section in the TOBY-L2 Data Sheet [1] or in the MPCI-L2 Data Sheet [2].</td>
<td>The modules may switch off if the supply voltage drops below the extended operating range minimum limit.</td>
</tr>
<tr>
<td>VCC or 3.3Vaux average current</td>
<td>Support with adequate margin the highest averaged current consumption value in connected-mode conditions specified for VCC in TOBY-L2 Data Sheet [1] or specified for 3.3Vaux in MPCI-L2 Data Sheet [2].</td>
<td>The maximum average current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and supply voltage. Sections 1.5.1.2, 1.5.1.3 and 1.5.1.4 describe current consumption profiles in 2G, 3G and LTE connected-mode.</td>
</tr>
<tr>
<td>VCC or 3.3Vaux peak current</td>
<td>Support with margin the highest peak current consumption value in 2G connected-mode conditions specified for VCC in TOBY-L2 Data Sheet [1] or specified for 3.3Vaux in MPCI-L2 Data Sheet [2].</td>
<td>The specified maximum peak of current consumption occurs during GSM single transmit slot in 850/900 MHz connected-mode, in case of mismatched antenna. Section 1.5.1.2 describes 2G Tx peak/pulse current.</td>
</tr>
<tr>
<td>VCC or 3.3Vaux voltage drop during 2G Tx slots</td>
<td>Lower than 400 mV</td>
<td>Supply voltage drop values greater than recommended during 2G TDMA transmission slots directly affect the RF compliance with applicable certification schemes. Figure 5 describes supply voltage drop during 2G Tx slots.</td>
</tr>
<tr>
<td>VCC or 3.3Vaux voltage ripple during RF transmission</td>
<td>Noise in the supply has to be minimized</td>
<td>High supply voltage ripple values during LTE/3G/2G RF transmissions in connected-mode directly affect the RF compliance with applicable certification schemes. Figure 5 describes supply voltage ripple during RF Tx.</td>
</tr>
<tr>
<td>VCC or 3.3Vaux under/over-shoot at start/end of Tx slots</td>
<td>Absent or at least minimized</td>
<td>Supply voltage under-shoot or over-shoot at the start or the end of 2G TDMA transmission slots directly affect the RF compliance with applicable certification schemes. Figure 5 describes supply voltage under/over-shoot.</td>
</tr>
</tbody>
</table>

Table 7: Summary of VCC or 3.3Vaux modules supply requirements
1.5.1.2 VCC or 3.3Vaux current consumption in 2G connected-mode

When a GSM call is established, the VCC or 3.3Vaux module current consumption is determined by the current consumption profile typical of the GSM transmitting and receiving bursts.

The peak of current consumption during a transmission slot is strictly dependent on the RF transmitted power, which is regulated by the network (the current base station). The transmitted power in the transmit slot is also the more relevant factor for determining the average current consumption.

If the module is transmitting in 2G single-slot mode in the 850 or 900 MHz bands, at the maximum RF power level (approximately 2 W or 33 dBm in the allocated transmit slot/burst) the current consumption can reach a high peak (see the “Current consumption” section in the TOBY-L2 Data Sheet [1] or the MPCI-L2 Data Sheet [2]) for 576.9 µs (width of the transmit slot/burst) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/burst), so with a 1/8 duty cycle according to GSM TDMA (Time Division Multiple Access).

If the module is transmitting in 2G single-slot mode in the 1800 or 1900 MHz bands, the current consumption figures are quite less high than the one in the low bands, due to 3GPP transmitter output power specifications. During a GSM call, current consumption is not so significantly high in receiving or in monitor bursts and is low in the inactive unused bursts.

Figure 4 shows an example of the module current consumption profile versus time in 2G single-slot mode.

![Current Consumption Profile](image1)

Figure 4: VCC or 3.3Vaux current consumption profile versus time during a 2G single-slot call (1 TX slot, 1 RX slot)

Figure 5 illustrates VCC or 3.3Vaux voltage profile versus time during a 2G single-slot call, according to the relative VCC or 3.3Vaux current consumption profile described in Figure 4.

![Voltage Profile](image2)

Figure 5: VCC or 3.3Vaux voltage profile versus time during a 2G single-slot call (1 TX slot, 1 RX slot)
When a GPRS connection is established, more than one slot can be used to transmit and/or more than one slot can be used to receive. The transmitted power depends on network conditions, which set the peak current consumption, but following the 3GPP specifications the maximum Tx RF power is reduced if more than one slot is used to transmit, so the maximum peak of current is not as high as can be in case of a 2G single-slot call.

The multi-slot transmission power can be further reduced by configuring the actual Multi-Slot Power Reduction profile with the dedicated AT command, AT+UDCONF=40 (see the u-blox AT Commands Manual [3]). This command is not supported by “00” and “60” product versions.

If the module transmits in GPRS class 12 in the 850 or 900 MHz bands, at the maximum RF power control level, the current consumption can reach a quite high peak but lower than the one achievable in 2G single-slot mode. This happens for 2.307 ms (width of the 4 transmit slots/bursts) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/bursts), so with a 1/2 duty cycle, according to 2G TDMA.

If the module is in GPRS connected mode in the 1800 or 1900 MHz bands, the current consumption figures are quite less high than the one in the low bands, due to 3GPP transmitter output power specifications.

Figure 6 reports the current consumption profiles in GPRS class 12 connected mode, in the 850 or 900 MHz bands, with 4 slots used to transmit and 1 slot used to receive.

![Figure 6: VCC or 3.3Vaux current consumption profile during a 2G GPRS/EDGE multi-slot connection (4 TX slots, 1 RX slot)](image)

In case of EDGE connections the VCC current consumption profile is very similar to the GPRS current profile, so the image shown in Figure 6, representing the current consumption profile in GPRS class 12 connected mode, is valid for the EDGE class 12 connected mode as well.
1.5.1.3 VCC or 3.3Vaux current consumption in 3G connected mode

During a 3G connection, the module can transmit and receive continuously due to the Frequency Division Duplex (FDD) mode of operation with the Wideband Code Division Multiple Access (WCDMA).

The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. These power control commands are logically divided into a slot of 666 µs, thus the rate of power change can reach a maximum rate of 1.5 kHz.

There are no high current peaks as in the 2G connection, since transmission and reception are continuously enabled due to FDD WCDMA implemented in the 3G that differs from the TDMA implemented in the 2G case.

In the worst scenario, corresponding to a continuous transmission and reception at maximum output power (approximately 250 mW or 24 dBm), the average current drawn by the module at the VCC pins is considerable (see the “Current consumption” section in TOBY-L2 Data Sheet [1] or in MPCI-L2 Data Sheet [2]). At the lowest output RF power (approximately 0.01 µW or –50 dBm), the current drawn by the internal power amplifier is strongly reduced. The total current drawn by the module at the VCC pins is due to baseband processing and transceiver activity.

Figure 7 shows an example of current consumption profile of the module in 3G WCDMA/DC-HSPA+ continuous transmission mode.

**Figure 7:** VCC or 3.3Vaux current consumption profile versus time during a 3G connection (TX and RX continuously enabled)
1.5.1.4 VCC or 3.3Vaux current consumption in LTE connected-mode

During an LTE connection, the module can transmit and receive continuously due to the Frequency Division Duplex (FDD) mode of operation used in LTE radio access technology.

The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. These power control commands are logically divided into a slot of 0.5 ms (time length of one Resource Block), thus the rate of power change can reach a maximum rate of 2 kHz.

The current consumption profile is similar to that in 3G radio access technology. Unlike the 2G connection mode, which uses the TDMA mode of operation, there are no high current peaks since transmission and reception are continuously enabled in FDD.

In the worst scenario, corresponding to a continuous transmission and reception at maximum output power (approximately 250 mW or 24 dBm), the average current drawn by the module at the VCC pins is considerable (see the “Current consumption” section in TOBY-L2 Data Sheet [1] or in MPCI-L2 Data Sheet [2]). At the lowest output RF power (approximately 0.01 µW or −50 dBm), the current drawn by the internal power amplifier is strongly reduced and the total current drawn by the module at the VCC pins is due to baseband processing and transceiver activity.

Figure 8 shows an example of the module current consumption profile versus time in LTE connected-mode. Detailed current consumption values can be found in TOBY-L2 Data Sheet [1] and in MPCI-L2 Data Sheet [2].

![Figure 8: VCC or 3.3Vaux current consumption profile versus time during LTE connection (TX and RX continuously enabled)](image-url)
1.5.1.5 **VCC or 3.3Vaux current consumption in cyclic idle/active mode (power saving enabled)**

The power saving configuration is by default disabled, but it can be enabled using the AT+UPSV command (see the u-blox AT Commands Manual [3]). When power saving is enabled, the module automatically enters the low power idle-mode whenever possible, reducing current consumption.

During low power idle-mode, the module processor runs with 32 kHz reference clock frequency.

When the power saving configuration is enabled and the module is registered or attached to a network, the module automatically enters the low power idle-mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance to the 2G/3G/LTE system requirements, even if connected-mode is not enabled by the application. When the module monitors the paging channel, it wakes up to the active-mode, to enable the reception of paging block. In between, the module switches to low power idle-mode. This is known as discontinuous reception (DRX).

The module processor core is activated during the paging block reception, and automatically switches its reference clock frequency from 32 kHz to the 26 MHz used in active-mode. The time period between two paging block receptions is defined by the network. This is the paging period parameter, fixed by the base station through broadcast channel sent to all users on the same serving cell:

- In case of 2G radio access technology, the paging period can vary from 470.8 ms (DRX = 2, length of 2 x 51 2G frames = 2 x 51 x 4.615 ms) up to 2118.4 ms (DRX = 9, length of 9 x 51 2G frames = 9 x 51 x 4.615 ms)
- In case of 3G radio access technology, the paging period can vary from 640 ms (DRX = 6, i.e. length of 2^6 3G frames = 64 x 10 ms) up to 5120 ms (DRX = 9, length of 2^7 3G frames = 512 x 10 ms).
- In case of LTE radio access technology, the paging period can vary from 320 ms (DRX = 5, i.e. length of 2^5 LTE frames = 32 x 10 ms) up to 2560 ms (DRX = 8, length of 2^8 LTE frames = 256 x 10 ms).

Figure 9 illustrates a typical example of the module current consumption profile when power saving is enabled.

The module is registered with network, automatically enters the low power idle-mode and periodically wakes up to active-mode to monitor the paging channel for the paging block reception. Detailed current consumption values can be found in TOBY-L2 Data Sheet [1] and in MPCI-L2 Data Sheet [2].

![Figure 9: VCC or 3.3Vaux current consumption profile with power saving enabled and module registered with the network: the module is in idle-mode and periodically wakes up to active-mode to monitor the paging channel for paging block reception](image-url)
1.5.1.6 VCC or 3.3Vaux current consumption in fixed active-mode (power saving disabled)

When power saving is disabled, the module does not automatically enter the low power idle-mode whenever possible: the module remains in active-mode. Power saving configuration is by default disabled. It can also be disabled using the AT+UPSV command (see u-blox AT Commands Manual [3] for detail usage).

The module processor core is activated during idle-mode, and the 26 MHz reference clock frequency is used. It would draw more current during the paging period than that in the power saving mode. Figure 10 illustrates a typical example of the module current consumption profile when power saving is disabled. In such case, the module is registered with the network and while active-mode is maintained, the receiver is periodically activated to monitor the paging channel for paging block reception. Detailed current consumption values can be found in TOBY-L2 Data Sheet [1] and in MPCI-L2 Data Sheet [2].

![Figure 10: VCC or 3.3Vaux current consumption profile with power saving disabled and module registered with the network: active-mode is always held and the receiver is periodically activated to monitor the paging channel for paging block reception](image-url)
1.5.2 RTC supply input/output (V_BCKP)

The RTC supply V_BCKP pin is not available on MPCI-L2 series modules.

The V_BCKP pin of TOBY-L2 series modules connects the supply for the Real Time Clock (RTC). A linear LDO regulator integrated in the Power Management Unit internally generates this supply, as shown in Figure 11, with low current capability (see the TOBY-L2 series Data Sheet [1]). The output of this regulator is always enabled when the main module voltage supply applied to the VCC pins is within the valid operating range.

![Figure 11: TOBY-L2 series RTC supply (V_BCKP) simplified block diagram](image)

The RTC provides the module time reference (date and time) that is used to set the wake-up interval during the low power idle-mode periods, and is able to make available the programmable alarm functions.

The RTC functions are available also in power-down mode when the V_BCKP voltage is within its valid range (specified in the “Input characteristics of Supply/Power pins” table in TOBY-L2 series Data Sheet [1]). The RTC can be supplied from an external back-up battery through the V_BCKP, when the main module voltage supply is not applied to the VCC pins. This lets the time reference (date and time) run until the V_BCKP voltage is within its valid range, even when the main supply is not provided to the module.

Consider that the module cannot switch on if a valid voltage is not present on VCC even when the RTC is supplied through V_BCKP (meaning that VCC is mandatory to switch on the module).

The RTC has very low current consumption, but is highly temperature dependent. For example, V_BCKP current consumption at the maximum operating temperature can be higher than the typical value at 25 °C specified in the “Input characteristics of Supply/Power pins” table in the TOBY-L2 series Data Sheet [1].

If V_BCKP is left unconnected and the module main supply is not applied to the VCC pins, the RTC is supplied from the bypass capacitor mounted inside the module. However, this capacitor is not able to provide a long buffering time: within few milliseconds the voltage on V_BCKP will go below the valid range (1.4 V min). This has no impact on cellular connectivity, as all the module functionalities do not rely on date and time setting.
1.5.3 Generic digital interfaces supply output (V\_INT)

The generic digital interfaces supply V\_INT pin is not available on MPCI-L2 series modules.

The V\_INT output pin of the TOBY-L2 series modules is connected to an internal 1.8 V supply with current capability specified in the TOBY-L2 series Data Sheet [1]. This supply is internally generated by a switching step-down regulator integrated in the Power Management Unit and it is internally used to source the generic digital I/O interfaces of the TOBY-L2 module, as described in Figure 12. The output of this regulator is enabled when the module is switched on and it is disabled when the module is switched off.

![Figure 12: TOBY-L2 series generic digital interfaces supply output (V\_INT) simplified block diagram](image)

The switching regulator operates in Pulse Width Modulation (PWM) mode for greater efficiency at high output loads and it automatically switches to Pulse Frequency Modulation (PFM) power save mode for greater efficiency at low output loads. The V\_INT output voltage ripple is specified in the TOBY-L2 series Data Sheet [1].
1.6  System function interfaces

1.6.1  Module power-on

The PWR_ON input pin is not available on MPCI-L2 series modules.

When the TOBY-L2 and MPCI-L2 series modules are in the not-powered mode (switched off, i.e. the VCC or 3.3Vaux module supply is not applied), they can be switched on as following:

- Rising edge on the VCC or 3.3Vaux supply input to a valid voltage for module supply, starting from a voltage value lower than 2.25 V, so that the module switches on applying a proper VCC or 3.3Vaux supply within the normal operating range.
- Alternately, the RESET_N or PERST# pin can be held to the low level during the VCC or 3.3Vaux rising edge, so that the module switches on releasing the RESET_N or PERST# pin when the VCC or 3.3Vaux module supply voltage stabilizes at its proper nominal value within the normal operating range.

The status of the PWR_ON input pin of TOBY-L2 modules while applying the VCC module supply is not relevant: during this phase the PWR_ON pin can be set high or low by the external circuit.

When the TOBY-L2 modules are in the power-off mode (i.e. switched off with valid VCC module supply applied), they can be switched on as following:

- Low level on the PWR_ON pin, which is normally set high by an internal pull-up, for a valid time period.
- Low level on the RESET_N pin, which is normally set high by an internal pull-up, for a valid time period.
- RTC alarm, i.e. pre-programmed alarm by AT+CALA command (see u-blox AT Commands Manual [3]).

As described in Figure 13, the TOBY-L2 series PWR_ON input is equipped with an internal active pull-up resistor to the VCC module supply: the PWR_ON input voltage thresholds are different from the other generic digital interfaces. Detailed electrical characteristics are described in TOBY-L2 series Data Sheet [1].

![Figure 13: TOBY-L2 series PWR_ON input description](image-url)
Figure 14 shows the module power-on sequence from the not-powered mode, describing the following phases:

- The external supply is applied to the VCC or 3.3Vaux module supply inputs, representing the start-up event.
- The PWR_ON and the RESET_N or PERST# pins suddenly rise to high logic level due to internal pull-ups.
- The V_BCKP RTC supply output is suddenly enabled by the module as VCC reaches a valid voltage value.
- All the generic digital pins of the module are tri-stated until the switch-on of their supply source (V_INT).
- The internal reset signal is held low: the baseband core and all the digital pins are held in the reset state. The reset state of all the digital pins is reported in the pin description table of TOBY-L2 Series Data Sheet [1].
- When the internal reset signal is released, any digital pin is set in a proper sequence from the reset state to the default operational configured state. The duration of this pins’ configuration phase differs within generic digital interfaces and the USB interface due to host / device enumeration timings (see section 1.9.1).
- The module is fully ready to operate after all interfaces are configured.

<table>
<thead>
<tr>
<th>Event</th>
<th>Start-up event</th>
<th>Start of interface configuration</th>
<th>Module interfaces are configured</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC or 3.3Vaux</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_BCKP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWR_ON</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESET_N or PERST#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_INT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal Reset</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>System State</td>
<td>OFF</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td>BB Pads State</td>
<td>Tristate / Floating</td>
<td>Internal Reset → Operational</td>
<td>Operational</td>
</tr>
</tbody>
</table>

![Power-on sequence diagram](image)

Figure 14: TOBY-L2 and MPCI-L2 series power-on sequence description

The greeting text can be activated by means of +CSGT AT command (see u-blox AT Commands Manual [3]) to notify the external application that the module is ready to operate (i.e. ready to reply to AT commands) and the first AT command can be sent to the module, given that autobauding has to be disabled on the UART to let the module sending the greeting text: the UART has to be configured at fixed baud rate (the baud rate of the application processor) instead of the default autobauding, otherwise the module does not know the baud rate to be used for sending the greeting text (or any other URC) at the end of the internal boot sequence.

- The Internal Reset signal is not available on a module pin, but the host application can monitor:
  - The V_INT pin to sense the start of the TOBY-L2 module power-on sequence.
  - The USB interface to sense the start of the MPCI-L2 module power-on sequence: the module, as USB device, informs the host of the attach event via a reply on its status change pipe for proper bus enumeration process according to Universal Serial Bus Revision 2.0 specification [7].

Before the switch-on of the generic digital interface supply source (V_INT) of the module, no voltage driven by an external application should be applied to any generic digital interface of TOBY-L2 module.

Before the TOBY-L2 and MPCI-L2 series module is fully ready to operate, the host application processor should not send any AT command over the AT communication interfaces (USB, UART) of the module.

The duration of the TOBY-L2 and MPCI-L2 series modules’ switch-on routine can vary depending on the application / network settings and the concurrent module activities.
1.6.2  Module power-off

TOBY-L2 series can be properly switched off by:

- AT+CPWROFF command (see u-blox AT Commands Manual [3]). The current parameter settings are saved in the module’s non-volatile memory and a proper network detach is performed.

The MPCI-L2 series modules do not switch off by the AT+CPWROFF command as the TOBY-L2 modules, but the AT+CPWROFF command causes a reset (reboot) of the module due to the MPCI-L2 module’s internal configuration: the command stores the actual parameter settings in the non-volatile memory of MPCI-L2 modules and performs a network detach, with a subsequent reset (reboot) of the module.

An abrupt under-voltage shutdown occurs on TOBY-L2 and MPCI-L2 series modules when the VCC or 3.3Vaux module supply is removed. If this occurs, it is not possible to perform the storing of the current parameter settings in the module’s non-volatile memory or to perform the proper network detach.

It is highly recommended to avoid an abrupt removal of the VCC supply during TOBY-L2 modules normal operations: the power off procedure must be started by the AT+CPWROFF command, waiting the command response for a proper time period (see u-blox AT Commands Manual [3]), and then a proper VCC supply has to be held at least until the end of the modules’ internal power off sequence, which occurs when the generic digital interfaces supply output (V_INT) is switched off by the module.

It is highly recommended to avoid an abrupt removal of the 3.3Vaux supply during MPCI-L2 modules normal operations: the power off procedure must be started by setting the MPCI-L2 module in the halt mode by the AT+CFUN=127 command (which stores the actual parameter settings in the non-volatile memory of the module and performs a network detach), waiting the command response for a proper time period (see the u-blox AT Commands Manual [3]), and then the 3.3Vaux supply can be removed.

An abrupt hardware shutdown occurs on TOBY-L2 series modules when a low level is applied on the RESET_N pin for a specific time period. In this case, the current parameter settings are not saved in the module’s non-volatile memory and a proper network detach is not performed.

It is highly recommended to avoid an abrupt hardware shutdown of the module by forcing a low level on the RESET_N input pin during module normal operation: the RESET_N line should be set low only if reset or shutdown via AT commands fails or if the module does not reply to a specific AT command after a time period longer than the one defined in the u-blox AT Commands Manual [3].

An over-temperature or an under-temperature shutdown occurs on TOBY-L2 and MPCI-L2 series modules when the temperature measured within the cellular module reaches the dangerous area, if the optional Smart Temperature Supervisor feature is enabled and configured by the dedicated AT command. For more details see u-blox AT Commands Manual [3], +USTS AT command.

The Smart Temperature Supervisor feature is not supported by the “00”, “01”, “60” product versions.
Figure 15 describes the TOBY-L2 power-off sequence by means of AT+CPWROFF with the following phases:

- When the +CPWROFF AT command is sent, the module starts the switch-off routine.
- The module replies OK on the AT interface: the switch-off routine is in progress.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (V_INT), except the RTC supply (V_BCKP).
- Then, the module remains in power-off mode as long as a switch on event does not occur (e.g. applying a proper low level to the PWR_ON input, or applying a proper low level to the RESET_N input), and enters not-powered mode if the supply is removed from the VCC pins.

![Diagram](image1)

**Figure 15: TOBY-L2 series power-off sequence description**

The Internal Reset signal is not available on a module pin, but the application can monitor the V_INT pin to sense the end of the power-off sequence.

Figure 16 describes the MPCI-L2 power-off procedure with the following phases:

- When the AT+CFUN=127 command is issued, the module starts the halt mode setting routine.
- The module replies OK on the AT interface: after this, the module is set in the halt mode.
- Then, the module remains in the Halt mode and enters not-powered mode if the supply is removed from the 3.3Vaux pins.

![Diagram](image2)

**Figure 16: MPCI-L2 series power-off procedure description**

The duration of each phase in the TOBY-L2 and MPCI-L2 series modules’ switch-off routines can largely vary depending on the application / network settings and the concurrent module activities.
1.6.3 Module reset

TOBY-L2 and MPCI-L2 series modules can be properly reset (rebooted) by:
- AT+CFUN command (see u-blox AT Commands Manual [3]).

MPCI-L2 series modules can be additionally properly reset (rebooted) by:
- AT+CPWROFF command (see u-blox AT Commands Manual [3]): the behavior differs than TOBY-L2 series, as MPCI-L2 modules will reboot rather than remain switched off due to modules’ internal configuration.

In the cases listed above an “internal” or “software” reset of the module is executed: the current parameter settings are saved in the module’s non-volatile memory and a proper network detach is performed.

An abrupt hardware reset occurs on TOBY-L2 and MPCI-L2 series modules when a low level is applied on the RESET_N or PERST# input pin for a specific time period. In this case, the current parameter settings are not saved in the module’s non-volatile memory and a proper network detach is not performed.

It is highly recommended to avoid an abrupt hardware reset of the module by forcing a low level on the RESET_N or PERST# input during modules normal operation: the RESET_N or PERST# line should be set low only if reset or shutdown via AT commands fails or if the module does not provide a reply to a specific AT command after a time period longer than the one defined in the u-blox AT Commands Manual [3].

As described in Figure 17, the RESET_N and PERST# input pins are equipped with an internal pull-up to the VCC supply in the TOBY-L2 series and to the 3.3 V in the MPCI-L2 series.

Figure 17: TOBY-L2 and MPCI-L2 series RESET_N and PERST# input equivalent circuit description

For more electrical characteristics details see TOBY-L2 Data Sheet [1] and MPCI-L2 Data Sheet [2].

1.6.4 Module configuration selection by host processor

The HOST_SELECT0 and HOST_SELECT1 pins are not available on MPCI-L2 series modules.

The selection of the module configuration by the host application processor over the HOST_SELECT0 and HOST_SELECT1 pins is not supported by all the TOBY-L2 series modules product versions.

TOBY-L2 series modules include two input pins (HOST_SELECT0 and HOST_SELECT1) for the selection of the module configuration by the host application processor.
1.7 Antenna interface

1.7.1 Antenna RF interfaces (ANT1 / ANT2)

TOBY-L2 and MPCI-L2 series modules provide two RF interfaces for connecting the external antennas:

- The **ANT1** represents the primary RF input/output for transmission and reception of LTE/3G/2G RF signals.
  
  The **ANT1** pin of TOBY-L2 series modules has a nominal characteristic impedance of 50 Ω and must be connected to the primary Tx / Rx antenna through a 50 Ω transmission line to allow proper RF transmission and reception.

  The **ANT1** Hirose U.FL-R-SMT coaxial connector receptacle of MPCI-L2 series modules has a nominal characteristic impedance of 50 Ω and must be connected to the primary Tx / Rx antenna through a mated RF plug with a 50 Ω coaxial cable assembly to allow proper RF transmission and reception.

- The **ANT2** represents the secondary RF input for the reception of the LTE RF signals for the Down-Link MIMO 2 x 2 radio technology supported by TOBY-L2 and MPCI-L2 series modules as required feature for LTE category 4 UEs, and for the reception of the 3G RF signals for the Down-Link Rx diversity radio technology supported by TOBY-L2 and MPCI-L2 series modules as additional feature for 3G DC-HSDPA category 24 UEs.

  The **ANT2** pin of TOBY-L2 series modules has a nominal characteristic impedance of 50 Ω and must be connected to the secondary Rx antenna through a 50 Ω transmission line to allow proper RF reception.

  The **ANT2** Hirose U.FL-R-SMT coaxial connector receptacle of MPCI-L2 series modules has a nominal characteristic impedance of 50 Ω and must be connected to the secondary Rx antenna through a mated RF plug with a 50 Ω coaxial cable assembly to allow proper RF reception.

The Multiple Input Multiple Output (MIMO) radio technology is an essential component of LTE radio systems based on the use of multiple antennas at both the transmitter and receiver sides to improve communication performance and achieve highest possible bit rate. A MIMO m x n system consists of m transmit and n receive antennas, where the data to be transmitted is divided into m independent data streams. Note that the terms Input and Output refer to the radio channel carrying the signal, not to the devices having antennas, so that in the Down-Link MIMO 2 x 2 system supported by TOBY-L2 and MPCI-L2 series modules:

- The LTE data stream is divided into 2 independent streams by the Tx-antennas of the base station
- The cellular modules, at the receiver side, receives both LTE data streams by 2 Rx-antennas (ANT1 / ANT2)

![Figure 18: Description of the LTE Down-Link MIMO 2 x 2 radio technology supported by TOBY-L2 and MPCI-L2 series modules](image-url)
### 1.7.1.1 Antenna RF interfaces requirements

Table 8, Table 9 and Table 10 summarize the requirements for the antennas RF interfaces (ANT1 / ANT2). See section 2.4.1 for suggestions to properly design antennas circuits compliant with these requirements.

The antenna circuits affect the RF compliance of the device integrating TOBY-L2 and MPCI-L2 series modules with applicable required certification schemes (for more details see section 4). Compliance is guaranteed if the antenna RF interfaces (ANT1 / ANT2) requirements summarized in Table 8, Table 9 and Table 10 are fulfilled.

<table>
<thead>
<tr>
<th>Item</th>
<th>Requirements</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Impedance</td>
<td>50 Ω nominal characteristic impedance</td>
<td>The impedance of the antenna RF connection must match the 50 Ω impedance of the ANT1 port.</td>
</tr>
<tr>
<td>Frequency Range</td>
<td>See the TOBY-L2 series Data Sheet [1] and the MPCI-L2 series Data Sheet [2]</td>
<td>The required frequency range of the antenna connected to ANT1 port depends on the operating bands of the used cellular module and the used mobile network.</td>
</tr>
<tr>
<td>Return Loss</td>
<td>$S_{11} &lt; -10$ dB (VSWR &lt; 2:1) recommended $S_{11} &lt; -6$ dB (VSWR &lt; 3:1) acceptable</td>
<td>The Return loss or the $S_{11}$, as the VSWR, refers to the amount of reflected power, measuring how well the primary antenna RF connection matches the 50 Ω characteristic impedance of the ANT1 port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the ANT1 port over the operating frequency range, reducing as much as possible the amount of reflected power.</td>
</tr>
<tr>
<td>Efficiency</td>
<td>$&gt;-1.5$ dB ( &gt; 70% ) recommended</td>
<td>The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the ANT1 port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as Total Radiated Power (TRP) and the Total Isotropic Sensitivity (TIS), specified by applicable related certification schemes.</td>
</tr>
<tr>
<td>Maximum Gain</td>
<td>According to radiation exposure limits</td>
<td>The power gain of an antenna is the radiation efficiency multiplied by the directivity: the gain describes how much power is transmitted in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to ANT1 port must not exceed the herein stated value to comply with regulatory agencies radiation exposure limits. For additional info see sections 4.2.2 and/or 4.3.1</td>
</tr>
<tr>
<td>Input Power</td>
<td>$&gt; 33$ dBm ( &gt; 2 W )</td>
<td>The antenna connected to the ANT1 port must support with adequate margin the maximum power transmitted by the modules.</td>
</tr>
</tbody>
</table>

**Table 8: Summary of primary Tx/Rx antenna RF interface (ANT1) requirements**
### Impedance

- **Requirements**: 50 Ω nominal characteristic impedance
- **Remarks**: The impedance of the antenna RF connection must match the 50 Ω impedance of the ANT2 port.

### Frequency Range

- **Requirements**: See the TOBY-L2 series Data Sheet [1] and the MPCI-L2 series Data Sheet [2]
- **Remarks**: The required frequency range of the antennas connected to ANT2 port depends on the operating bands of the used cellular module and the used Mobile Network.

### Return Loss

- **Requirements**: $S_{11} < -10$ dB (VSWR < 2:1) recommended, $S_{11} < -6$ dB (VSWR < 3:1) acceptable
- **Remarks**: The Return loss or the $S_{11}$, as the VSWR, refers to the amount of reflected power, measuring how well the secondary antenna RF connection matches the 50 Ω characteristic impedance of the ANT2 port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the ANT2 port over the operating frequency range, reducing as much as possible the amount of reflected power.

### Efficiency

- **Requirements**: $> -1.5$ dB ( > 70% ) recommended, $> -3.0$ dB ( > 50% ) acceptable
- **Remarks**: The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the ANT2 port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as the TIS, specified by applicable related certification schemes.

### Table 9: Summary of secondary Rx antenna RF interface (ANT2) requirements

<table>
<thead>
<tr>
<th>Item</th>
<th>Requirements</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency imbalance</td>
<td>$&lt; 0.5$ dB recommended, $&lt; 1.0$ dB acceptable</td>
<td>The radiation efficiency imbalance is the ratio of the primary (ANT1) antenna efficiency to the secondary (ANT2) antenna efficiency: the efficiency imbalance is a measure of how much better an antenna receives or transmits compared to the other antenna. The radiation efficiency of the secondary antenna needs to be roughly the same of the radiation efficiency of the primary antenna for good RF performance.</td>
</tr>
<tr>
<td>Envelope Correlation Coefficient</td>
<td>$&lt; 0.4$ recommended, $&lt; 0.5$ acceptable</td>
<td>The Envelope Correlation Coefficient (ECC) between the primary (ANT1) and the secondary (ANT2) antenna is an indicator of 3D radiation pattern similarity between the two antennas: low ECC results from antenna patterns with radiation lobes in different directions. The ECC between primary and secondary antenna needs to be enough low to comply with radiated performance requirements specified by related certification schemes.</td>
</tr>
<tr>
<td>Isolation</td>
<td>$&gt; 15$ dB recommended, $&gt; 10$ dB acceptable</td>
<td>The antenna to antenna isolation is the loss between the primary (ANT1) and the secondary (ANT2) antenna: high isolation results from low coupled antennas. The isolation between primary and secondary antenna needs to be high for good RF performance.</td>
</tr>
</tbody>
</table>

### Table 10: Summary of primary (ANT1) and secondary (ANT2) antennas relationship requirements
1.7.2 Antenna detection interface (ANT_DET)

Antenna detection (ANT_DET) is not available on MPCI-L2 series modules.

Antenna detection (ANT_DET) is not supported by TOBY-L2 “00”, “01” and “60” product versions.

The antenna detection is based on ADC measurement. The ANT_DET pin is an Analog to Digital Converter (ADC) provided to sense the antenna presence.

The antenna detection function provided by ANT_DET pin is an optional feature that can be implemented if the application requires it. The antenna detection is forced by the +UANTR AT command. See the u-blox AT Commands Manual [3] for more details on this feature.

The ANT_DET pin generates a DC current (for detailed characteristics see the TOBY-L2 series Data Sheet [1]) and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. So, the requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 2.4.2 for antenna detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

1.8 SIM interface

1.8.1 SIM interface

TOBY-L2 and MPCI-L2 series modules provide high-speed SIM/ME interface including automatic detection and configuration of the voltage required by the connected SIM card or chip.

Both 1.8 V and 3 V SIM types are supported. Activation and deactivation with automatic voltage switch from 1.8 V to 3 V are implemented, according to ISO-IEC 7816-3 specifications. The VSIM or UIM_PWR supply output provides internal short circuit protection to limit start-up current and protect the SIM to short circuits.

The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values determined by the SIM card or chip.

1.8.2 SIM detection interface

SIM detection (GPIO5) is not available on MPCI-L2 series modules.

SIM detection (GPIO5) is not supported by TOBY-L2 “00”, “01” and “60” product versions.

The GPIO5 pin is by default configured to detect the external SIM card mechanical / physical presence. The pin is configured as input, and it can sense SIM card presence as intended to be properly connected to the mechanical switch of a SIM card holder as described in section 2.5:

- Low logic level at GPIO5 input pin is recognized as SIM card not present
- High logic level at GPIO5 input pin is recognized as SIM card present

The SIM card detection function provided by GPIO5 pin is an optional feature that can be implemented / used or not according to the application requirements: an Unsolicited Result Code (URC) is generated each time that there is a change of status (for more details see u-blox AT Commands Manual [3], +UGPIOC, +CIND, +CMER).

The optional function “SIM card hot insertion/removal” can be additionally enabled on the GPIO5 pin by specific AT command (see the u-blox AT Commands Manual [3], +UDCONF=50), to enable / disable the SIM interface upon detection of external SIM card physical insertion / removal.
1.9 Data communication interfaces

TOBY-L2 and MPCI-L2 series modules provide the following serial communication interface:

- **USB interface:** High-Speed USB 2.0 compliant interface available for the communication with an external host application processor, for AT commands, data communication, FW upgrade by means of the FOAT feature, FW upgrade by means of the u-blox EasyFlash tool and for diagnostic purpose (see section 1.9.1 for functional description)

TOBY-L2 series modules additionally provide the following serial communication interfaces:

- **UART interface:** asynchronous serial interface available for the communication with an external host application processor, for AT commands, data communication, FW upgrade by means of the FOAT feature (see section 1.9.2 for functional description)
- **DDC interface:** i2C bus compatible interface available for the communication with external i2C devices as an audio codec (see section 1.9.3 for functional description)
- **SDIO interface:** Secure Digital Input Output interface available for the communication with an external u-blox Wi-Fi module (see section 1.9.4 for functional description)

1.9.1 Universal Serial Bus (USB)

1.9.1.1 USB features

TOBY-L2 and MPCI-L2 series modules include a High-Speed USB 2.0 compliant interface with maximum data rate of 480 Mb/s, representing the main interface for transferring high speed data with a host application processor: the USB interface is available for AT commands, data communication, FW upgrade by means of the FOAT feature, FW upgrade by means of the u-blox EasyFlash tool and for diagnostic purpose.

The module itself acts as a USB device and can be connected to a USB host such as a Personal Computer or an embedded application microprocessor equipped with compatible drivers.

The USB_D+ / USB_D- lines carry the USB serial bus data and signaling, providing all the functionalities for the bus attachment, configuration, enumeration, suspension or remote wakeup according to the Universal Serial Bus Revision 2.0 specification [7].

The **VUSB_DET** functionality is not supported by all the TOBY-L2 modules product versions: the pin should be left unconnected or it should not be driven high by any external device, because a high logic level applied to the pin will represent a module switch-on event (additional to the ones listed in section 1.6.1) and will prevent reaching the minimum possible consumption with power saving enabled.

The **VUSB_DET** pin is not available on MPCI-L2 series modules.

The USB interface is controlled and operated with:

- AT commands according to 3GPP TS 27.007 [9], 3GPP TS 27.005 [10], 3GPP TS 27.010 [11]
- u-blox AT commands

For the complete list of supported AT commands and their syntax see u-blox AT Commands Manual [3].
TOBY-L2 and MPCI-L2 modules provide by default the following USB profile with the listed set of USB functions:

- 1 RNDIS for Ethernet-over-USB connection
- 1 CDC-ACM for AT commands and data communication

The USB profile of TOBY-L2 and MPCI-L2 modules identifies itself by its VID (Vendor ID) and PID (Product ID) combination, included in the USB device descriptor according to the USB 2.0 specifications [7].

The VID and PID of the default USB profile configuration with the set of functions described above (1 RNDIS for Ethernet-over-USB, and 1 CDC-ACM for AT commands and data) are the following:

- VID = 0x1546
- PID = 0x1146

Figure 19 summarizes the USB end-points available with the default USB profile configuration.

The USB of the modules can be configured by the AT+UUSBCONF command (for more details see the u-blox AT Commands Manual [3]) to select different sets of USB functions available in mutually exclusive way, selecting the active USB profile consisting of a specific set of functions with various capabilities and purposes, such as:

- CDC-ACM for AT commands and data
- CDC-ACM for remote SIM Access Profile (SAP)\(^9\)
- CDC-ACM for diagnostic
- RNDIS for Ethernet-over-USB
- CDC-ECM for Ethernet-over-USB

\(^9\) Not supported by “00”, “01”, “02”, “60”, “62” product versions
For example, the default USB profile configuration which provides 2 functions (1 RNDIS for Ethernet-over-USB, and 1 CDC-ACM for AT commands and data) can be changed by means of the AT+UUSBCONF command switching to a USB profile configuration which provides the following 6 functions:

- 3 CDC-ACM for AT commands and data
- 1 CDC-ACM for GNSS tunneling
- 1 CDC-ACM for remote SIM Access Profile (SAP)
- 1 CDC-ACM for diagnostic

As each USB profile of TOBY-L2 and MPCI-L2 modules identifies itself by its specific VID and PID combination included in the USB device descriptor according to the USB 2.0 specifications, the VID and PID combination changes as following by switching the active USB profile configuration to the set of functions described above (3 CDC-ACM for AT commands and data, and 1 CDC-ACM for diagnostic):

- VID = 0x1546
- PID = 0x1141

Alternatively, as another example, the USB profile configuration can be changed by means of the AT+UUSBCONF command switching to a USB profile configuration which provides the following functions:

- 1 CDC-ECM for Ethernet-over-USB
- 3 CDC-ACM for AT commands and data

In case of this USB profile with the set of functions described above (1 CDC-ECM for Ethernet-over-USB, and 3 CDC-ACM for AT commands and data), the VID and PID are the following:

- VID = 0x1546
- PID = 0x1143

The switch of the active USB profile selected by the AT+UUSBCONF command is not performed immediately. The settings are saved in the non-volatile memory of the module at the power off, triggered by means of the AT+CPWROFF command, and the new configuration is effective at the subsequent reboot of the module.

If the USB is connected to the host before the module is switched on, or if the module is reset (rebooted) with the USB connected to the host, the VID and PID are automatically updated during the boot of the module. First, VID and PID are the following:

- VID = 0x1546
- PID = 0x1140

This VID and PID combination identifies a USB profile where no USB function described above is available: AT commands must not be sent to the module over the USB profile identified by this VID and PID combination. Then, after a time period (roughly 20 s, depending on the host / device enumeration timings), the VID and PID are updated to the ones related to the USB profile selected by the AT+UUSBCONF command.

For more details regarding the TOBY-L2 and MPCI-L2 series modules USB configurations and capabilities, see the u-blox AT Commands Manual [3], +UUSCONF AT command.

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10 Not supported by “00”, “01”, “02”, “03”, “60”, “62” product versions

11 Not supported by “00”, “01”, “02”, “60”, “62” product versions
1.9.1.2 **USB in Windows**

USB drivers are provided for Windows operating system platforms and should be properly installed / enabled by following the step-by-step instructions available in the EVK-L2x User Guide [4] or in the Windows Embedded OS USB Driver Installation Application Note [5].

USB drivers are available for the following operating system platforms:

- Windows Vista
- Windows 7
- Windows 8
- Windows 8.1
- Windows 10
- Windows Embedded CE 6.0
- Windows Embedded Compact 7
- Windows Embedded Compact 2013

The module firmware can be upgraded over the USB interface by means of the FOAT feature, or using the u-blox EasyFlash tool (for more details see Firmware Update Application Note [6]).

1.9.1.3 **USB in Linux/Android**

It is not required to install a specific driver for each Linux-based or Android-based operating system (OS) to use the module USB interface, which is compatible with standard Linux/Android USB kernel drivers.

The full capability and configuration of the module USB interface can be reported by running “lsusb –v” or an equivalent command available in the host operating system when the module is connected.

1.9.1.4 **USB and power saving**

The modules automatically enter the USB suspended state when the device has observed no bus traffic for a specific time period according to the USB 2.0 specification [7]. In suspended state, the module maintains any USB internal status as device. In addition, the module enters the suspended state when the hub port it is attached to is disabled. This is referred to as USB selective suspend.

If the USB is suspended and a power saving configuration is enabled by the AT+UPSV command, the module automatically enters the low power idle-mode whenever possible but it wakes up to active-mode according to any required activity related to the network (e.g. the periodic paging reception described in section 1.5.1.5) or any other required activity related to the functions / interfaces of the module.

The USB exits suspend mode when there is bus activity. If the USB is connected and not suspended, the module is forced to stay in active-mode, therefore the AT+UPSV settings are overruled but they have effect on the power saving configuration of the other interfaces.

The modules are capable of USB remote wake-up signaling: i.e. it may request the host to exit suspend mode or selective suspend by using electrical signaling to indicate remote wake-up, for example due to incoming call, UR Cs, data reception on a socket. The remote wake-up signaling notifies the host that it should resume from its suspended mode, if necessary, and service the external event. Remote wake-up is accomplished using electrical signaling described in the USB 2.0 specifications [7].

For the module current consumption description with power saving enabled and USB suspended, or with power saving disabled and USB not suspended, see the sections 1.5.1.5, 1.5.1.6 and the TOBY-L2 Data Sheet [1] or the MPCI-L2 Data Sheet [2].
1.9.2 Asynchronous serial interface (UART)

The UART interface is not available on MPCI-L2 series modules.

The UART interface is not supported by TOBY-L2 series modules “00” product versions.

1.9.2.1 UART features

The UART interface is a 9-wire 1.8 V unbalanced asynchronous serial interface (UART) that can be connected to an application host processor for AT commands and data communication.

The module firmware can be upgraded over the UART interface by means of the Firmware upgrade over AT (FOAT) feature only: for more details see section 1.15 and Firmware Update Application Note [6].

UART interface provides RS-232 functionality conforming to the ITU-T V.24 Recommendation [8], with CMOS compatible signal levels: 0 V for low data bit or ON state, and 1.8 V for high data bit or OFF state (for detailed electrical characteristics see TOBY-L2 Data Sheet [1]), providing:

- data lines (RXD as output, TXD as input),
- hardware flow control lines (CTS as output, RTS as input),
- modem status and control lines (DTR as input, DSR as output, DCD as output, RI as output).

TOBY-L2 modules are designed to operate as LTE/3G/2G cellular modems, i.e. as the data circuit-terminating equipment (DCE) according to the ITU-T V.24 Recommendation [8]. A host application processor connected to the module through the UART interface represents the data terminal equipment (DTE).

UART signal names of TOBY-L2 modules conform to the ITU-T V.24 Recommendation [8]: e.g. TXD line represents data transmitted by the DTE (host processor output) and received by the DCE (module input).

The UART interface is controlled and operated with:

- AT commands according to 3GPP TS 27.007 [9], 3GPP TS 27.005 [10], 3GPP TS 27.010 [11]
- u-blox AT commands

For the complete list of supported AT commands and their syntax see u-blox AT Commands Manual [3], and in particular for the UART configuration see the +IPR, +ICF, +IFC, &K, \Q, +UPSV AT commands.

Flow control handshakes are supported by the UART interface and can be set by appropriate AT commands (see u-blox AT Commands Manual [3], &K, +IFC, \Q AT commands): hardware flow control (over the RTS / CTS lines), software flow control (XON/XOFF), or none flow control.

Hardware flow control is enabled by default.

Software flow control is not supported by “00”, “01”, “60” and TOBY-L201-02S product versions.

The one-shot autobauding is supported: the automatic baud rate detection is performed only once, at module start up. After the detection, the module works at the detected baud rate and the baud rate can only be changed by AT command (see u-blox AT Commands Manual [3], +IPR).

One-shot automatic baud rate recognition (autobauding) is enabled by default.
The following baud rates can be configured by AT command (see u-blox AT Commands Manual [3], +IPR):
- 9600 b/s
- 19200 b/s
- 38400 b/s
- 57600 b/s
- 115200 b/s, default value when one-shot autobauding is disabled
- 230400 b/s
- 460800 b/s
- 921600 b/s

The following frame formats can be configured by AT command (see u-blox AT Commands Manual [3], +ICF):
- 8N2 (8 data bits, no parity, 2 stop bits)
- 8N1 (8 data bits, no parity, 1 stop bit), default frame format
- 8E1 (8 data bits, even parity, 1 stop bit)
- 8O1 (8 data bits, odd parity, 1 stop bit)
- 7N2 (7 data bits, no parity, 2 stop bits)
- 7N1 (7 data bits, no parity, 1 stop bit)
- 7E1 (7 data bits, even parity, 1 stop bit)
- 7O1 (7 data bits, odd parity, 1 stop bit)

Automatic frame recognition is not supported by all the TOBY-L2 modules product versions.

Figure 20 describes the 8N1 frame format, which is the default frame format configuration.

![Figure 20: Description of UART default frame format (8N1, i.e. 8 data bits, no parity, 1 stop bit)](image-url)
1.9.2.2 UART interface configuration

The UART interface of TOBY-L2 series modules is available as AT command interface with the default configuration described in Table 11 (for more details and information about further settings, see the u-blox AT Commands Manual [3]).

<table>
<thead>
<tr>
<th>Interface</th>
<th>AT Settings</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART interface</td>
<td>AT interface: enabled</td>
<td>AT command interface is enabled by default on the UART physical interface</td>
</tr>
<tr>
<td></td>
<td>AT+IPR=0</td>
<td>One-shot autobauding enabled by default on the modules</td>
</tr>
<tr>
<td></td>
<td>AT+ICF=3,1</td>
<td>8N1 frame format enabled by default</td>
</tr>
<tr>
<td></td>
<td>AT&amp;T&amp;K3</td>
<td>HW flow control enabled by default</td>
</tr>
<tr>
<td></td>
<td>AT&amp;S1</td>
<td>DSR line (Circuit 107 in ITU-T V.24) set ON in data mode and set OFF in command mode</td>
</tr>
<tr>
<td></td>
<td>AT&amp;D1</td>
<td>Upon an ON-to-OFF transition of DTR line (Circuit 108/2 in ITU-T V.24), the module (DCE) enters online command mode and issues an OK result code</td>
</tr>
<tr>
<td></td>
<td>AT&amp;C1</td>
<td>DCD line (Circuit 109 in ITU-T V.24) changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise</td>
</tr>
<tr>
<td></td>
<td>MUX protocol: disabled</td>
<td>Multiplexing mode is disabled by default and it can be enabled by AT+CMUX command. For more details, see the Mux Implementation Application Note [12]. The following virtual channels are defined:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Channel 0: control channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Channel 1 – 5: AT commands / data connection</td>
</tr>
</tbody>
</table>

Table 11: Default UART interface configuration

1.9.2.3 UART signals behavior

At the module switch-on, before the UART interface initialization (as described in the power-on sequence reported in Figure 14), each pin is first tri-stated and then is set to its relative internal reset state. At the end of the boot sequence, the UART interface is initialized, the module is by default in active-mode, and the UART interface is enabled as AT commands interface.

The configuration and the behavior of the UART signals after the boot sequence are described below. See section 1.4 for definition and description of module operating modes referred to in this section.

RXD signal behavior

The module data output line (RXD) is set by default to the OFF state (high level) at UART initialization. The module holds RXD in the OFF state until the module does not transmit some data.

TXD signal behavior

The module data input line (TXD) is set by default to the OFF state (high level) at UART initialization. The TXD line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the TXD input.

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12 For the definition of the interface data mode, command mode and online command mode see the u-blox AT Commands Manual [3]
13 See the pin description table in the TOBY-L2 series Data Sheet [1]
**CTS signal behavior**

The module hardware flow control output (CTS line) is set to the ON state (low level) at UART initialization. If the hardware flow control is enabled, as it is by default, the CTS line indicates when the UART interface is enabled (data can be received): the module drives the CTS line to the ON state or to the OFF state when it is either able or not able to accept data from the DTE over the UART (for example see section 1.9.2.4, Figure 23).

The module guarantees the reception of characters when the CTS line is set to the ON state, and the module is also able to accept up to 3 characters after the CTS line is set to the OFF state.

If hardware flow control is enabled, then when the CTS line is OFF it does not necessarily mean that the module is in low power idle-mode, but only that the UART is not enabled, as the module could be forced to stay in active-mode for other activities, e.g. related to the network or related to other interfaces.

If hardware flow control is enabled and the multiplexer protocol is active, then the CTS line state is mapped to FCon / FCoFF MUX command for flow control matters outside the power saving configuration while the physical CTS line is still used as a UART power state indicator (see the Mux Implementation Application Note [12]).

The CTS hardware flow control setting can be changed by AT commands (for more details, see the u-blox AT Commands Manual [3], AT&K, ATQ, AT+IFC AT commands).

If the hardware flow control is not enabled, the CTS line still indicates when the UART interface is enabled, as it does when hardware flow control is enabled. The module drives the CTS line to the ON state or to the OFF state when it is either able or not able to accept data from the DTE over the UART interface.

When the power saving configuration is enabled by AT+UPSV command and the hardware flow-control is not implemented in the DTE/DCE connection, data sent by the DTE can be lost: the first character sent when the module is in low power idle-mode will not be a valid communication character (see section 1.9.2.4 and in particular the sub-section “Wake up via data reception” for further details).

**RTS signal behavior**

The hardware flow control input (RTS line) is set by default to the OFF state (high level) at UART initialization. The module then holds the RTS line in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the RTS input.

If the HW flow control is enabled, as it is by default, the module monitors the RTS line to detect permission from the DTE to send data to the DTE itself. If the RTS line is set to the OFF state, any on-going data transmission from the module is interrupted until the RTS line changes to the ON state.

The DTE must still be able to accept a certain number of characters after the RTS line is set to the OFF state: the module guarantees the transmission interruption within two characters from RTS state change.

The module behavior according to the RTS hardware flow control status can be configured by AT commands (for more details, see the u-blox AT Commands Manual [3], AT&K, ATQ, AT+IFC AT commands).

If AT+UPSV=2 is set and HW flow control is disabled, the module monitors the RTS line to manage the power saving configuration (for more details, see section 1.9.2.4 and u-blox AT Commands Manual [3], AT+UPSV):

- When an OFF-to-ON transition occurs on the RTS input, the UART is enabled and the module is forced to active-mode: after ~5 ms from the transition the switch is completed and data can be received without loss. The module cannot enter low power idle-mode and the UART is keep enabled as long as the RTS input line is held in the ON state.
- If the RTS input line is set to the OFF state by the DTE, the UART is disabled (held in low power mode) and the module automatically enters low power idle-mode whenever possible.
DSR signal behavior
If AT&S1 is set, as it is by default, the DSR module output line is set by default to the OFF state (high level) at UART initialization. The DSR line is then set to the OFF state when the module is in command mode\(^4\) or in online command mode\(^4\) and is set to the ON state when the module is in data mode\(^4\).

If AT&S0 is set, the DSR module output line is set by default to the ON state (low level) at UART initialization and is then always held in the ON state.

DTR signal behavior
The DTR module input line is set by default to the OFF state (high level) at UART initialization. The module then holds the DTR line in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the DTR input.

Module behavior according to DTR status can be changed by AT command configuration (for more details see the u-blox AT Commands Manual [3], &D AT command description).

If AT+UPSV=3 is set, the DTR line is monitored by the module to manage the power saving configuration (for more details, see section 1.9.2.4 and u-blox AT Commands Manual [3], AT+UPSV):
- When an OFF-to-ON transition occurs on the DTR input, the UART is enabled and the module is forced to active-mode; after ~5 ms from the transition, the switch is completed and data can be received without loss. The module cannot enter low power idle-mode and the UART is keep enabled as long as the DTR input line is held in the ON state
- If the DTR input line is set to the OFF state by the DTE, the UART is disabled (held in low power mode) and the module automatically enters low power idle-mode whenever possible

DCD signal behavior
If AT&C1 is set, as it is by default, the DCD module output line is set by default to the OFF state (high level) at UART initialization. The module then sets the DCD line according to the carrier detect status: ON if the carrier is detected, OFF otherwise.

In case of voice calls, DCD is set to the ON state when the call is established.

If a Packet Switched Data call occurs before activating the PPP protocol (data mode), a dial-up application must provide the ATD*99***<context_number> to the module: with this command the module switches from command mode\(^14\) to data mode\(^14\) and can accept PPP packets. The module sets the DCD line to the ON state, then answers with a CONNECT to confirm the ATD*99 command. The DCD ON is not related to the context activation but with the data mode.

The DCD is set to ON during the execution of the +CMGS, +CMGW, +USOWR, +USODL AT commands requiring input data from the DTE: the DCD line is set to the ON state as soon as the switch to binary/text input mode is completed and the prompt is issued; DCD line is set to OFF as soon as the input mode is interrupted or completed (for more details see the u-blox AT Commands Manual [3]).

The DCD line is kept in the ON state, even during the online command mode\(^14\), to indicate that the data call is still established even if suspended, while if the module enters command mode\(^14\), the DSR line is set to the OFF state. For more details see DSR signal behavior description.

For scenarios when the DCD line setting is requested for different reasons (e.g. SMS texting during online command mode\(^14\)), the DCD line changes to guarantee the correct behavior for all the scenarios. For example, in case of SMS texting in online command mode\(^14\), if the data call is released, DCD is kept ON till the SMS command execution is completed (even if the data call release would request DCD set OFF).

If AT&C0 is set, the DCD module output line is set by default to the ON state (low level) at UART initialization and is then always held in the ON state.

\(^4\) For the definition of the interface data mode, command mode and online command mode see the u-blox AT Commands Manual [3]
RI signal behavior

The **RI** module output line is set by default to the OFF state (high level) at UART initialization.

The **RI** line can notify an incoming call: the **RI** line is switched from the OFF state to the ON state with a 4:1 duty cycle and a 5 s period (ON for 1 s, OFF for 4 s, see Figure 21), until the DTE attached to the module sends the ATA string and the module accepts the incoming data call. The RING string sent by the module (DCE) to the serial port at constant time intervals is not correlated with the switch of the **RI** line to the ON state.

![Figure 21: RI behavior during an incoming call](image)

RI line incoming call notification is not supported by “00”, “01”, “60”, TOBY-L201-02S product versions.

The **RI** output line can notify an SMS arrival. When the SMS arrives, the **RI** line switches from OFF to ON for 1 s (see Figure 22), if the feature is enabled by AT+CNMI command (see the u-blox AT Commands Manual [3]).

![Figure 22: RI behavior at SMS arrival](image)

This behavior allows the DTE to stay in power saving mode until the DCE related event requests service.

For SMS arrival, if several events coincidently occur or in quick succession each event independently triggers the **RI** line, although the line will not be deactivated between each event. As a result, the **RI** line may stay to ON for more than 1 s, if an incoming call is answered within less than 1 s (with ATA or if auto-answering is set to ATS0=1) than the **RI** line is set to OFF earlier, so that:

- **RI** line monitoring cannot be used by the DTE to determine the number of received SMSes.
- For multiple events (incoming call plus SMS received), the **RI** line cannot be used to discriminate the two events, but the DTE must rely on subsequent URCs and interrogate the DCE with the proper commands.

The **RI** line can additionally notify all the URCs and/or all the incoming data in PPP and Direct Link connections, if the feature is enabled by the AT+URING command (for more details see the u-blox AT Commands Manual [3]): the **RI** line is asserted when one of the configured events occur and it remains asserted for 1 s unless another configured event will happen, with the same behavior described in Figure 22.

The AT+URING command for the notification of all the URCs and/or incoming data in PPP and Direct Link connections over **RI** line is not supported by “00”, “01”, “60”, TOBY-L201-02S product versions.
### 1.9.2.4 UART and power-saving

The power saving configuration is controlled by the AT+UPSV command (for the complete description, see the u-blox AT Commands Manual [3]). When power saving is enabled, the module automatically enters low power idle-mode whenever possible, and otherwise the active-mode is maintained by the module (see section 1.4 for definition and description of module operating modes referred to in this section).

The AT+UPSV command configures both the module power saving and also the UART behavior in relation to the power saving. The conditions for the module entering low power idle-mode also depend on the UART power saving configuration, as the module does not enter the low power idle-mode according to any required activity related to the network (within or outside an active call) or any other required concurrent activity related to the functions and interfaces of the module, including the UART interface.

The AT+UPSV command can set these different power saving configurations:

- **AT+UPSV=0**, power saving disabled (default configuration)
- **AT+UPSV=1**, power saving enabled cyclically
- **AT+UPSV=2**, power saving enabled and controlled by the UART RTS input line
- **AT+UPSV=3**, power saving enabled and controlled by the UART DTR input line

The different power saving configurations that can be set by the +UPSV AT command are described in details in the following subsections. Table 12 summarizes the UART interface communication process in the different power saving configurations, in relation with the hardware flow control settings and the RTS input line status. For more details on the +UPSV AT command description, see u-blox AT commands Manual [3].

<table>
<thead>
<tr>
<th>AT+UPSV</th>
<th>HW flow control</th>
<th>RTS line</th>
<th>DTR line</th>
<th>Communication during idle-mode and wake up</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Enabled (AT&amp;K3)</td>
<td>ON</td>
<td>ON or OFF</td>
<td>Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE.</td>
</tr>
<tr>
<td>0</td>
<td>Enabled (AT&amp;K3)</td>
<td>OFF</td>
<td>ON or OFF</td>
<td>Data sent by the DTE is correctly received by the module. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. RTS line will be ON).</td>
</tr>
<tr>
<td>0</td>
<td>Disabled (AT&amp;K0)</td>
<td>ON or OFF</td>
<td>ON or OFF</td>
<td>Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the module if it is ready to receive data, otherwise the data is lost.</td>
</tr>
<tr>
<td>1</td>
<td>Enabled (AT&amp;K3)</td>
<td>ON</td>
<td>ON or OFF</td>
<td>Data sent by the DTE is buffered by the DTE and will be correctly received by the module when it is ready to receive data (when the UART is enabled). Data sent by the module is correctly received by the DTE.</td>
</tr>
<tr>
<td>1</td>
<td>Enabled (AT&amp;K3)</td>
<td>OFF</td>
<td>ON or OFF</td>
<td>Data sent by the DTE is buffered by the DTE and will be correctly received by the module when it is ready to receive data (when the UART is enabled). Data sent by the module is correctly received by the module if it is ready to receive data (i.e. RTS line will be ON).</td>
</tr>
<tr>
<td>1</td>
<td>Disabled (AT&amp;K0)</td>
<td>ON or OFF</td>
<td>ON or OFF</td>
<td>The first character sent by the DTE is lost by the module, but after ~5 ms the UART and the module are woken up: recognition of subsequent characters is guaranteed only after the UART / module complete wake-up (i.e. after ~5 ms). Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise the data is lost.</td>
</tr>
<tr>
<td>2</td>
<td>Enabled (AT&amp;K3)</td>
<td>ON or OFF</td>
<td>ON or OFF</td>
<td>Not Applicable: HW flow control cannot be enabled with AT+UPSV=2.</td>
</tr>
<tr>
<td>2</td>
<td>Disabled (AT&amp;K0)</td>
<td>ON</td>
<td>ON or OFF</td>
<td>Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.</td>
</tr>
<tr>
<td>2</td>
<td>Disabled (AT&amp;K0)</td>
<td>OFF</td>
<td>ON or OFF</td>
<td>Data sent by the DTE is lost by the module(^{15}). Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.</td>
</tr>
</tbody>
</table>

\(^{15}\) Only the first character sent by the DTE is lost by ‘01’, ‘60’, TOBY-L201-02S product versions: the UART and the module are woken up after ~5 ms due to wake up via data reception, and recognition of subsequent characters is guaranteed after the UART / module wake-up.
### AT+UPSV: UART and power-saving summary

<table>
<thead>
<tr>
<th>AT+UPSV</th>
<th>HW flow control</th>
<th>RTS line</th>
<th>DTR line</th>
<th>Communication during idle-mode and wake up</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Enabled (AT&amp;K3)</td>
<td>ON</td>
<td>ON</td>
<td>Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE.</td>
</tr>
<tr>
<td>3</td>
<td>Enabled (AT&amp;K3)</td>
<td>ON</td>
<td>OFF</td>
<td>Data sent by the DTE is buffered by the DTE and will be correctly received by the module when it is ready to receive data (when the UART is enabled). Data sent by the module is correctly received by the DTE.</td>
</tr>
<tr>
<td>3</td>
<td>Enabled (AT&amp;K3)</td>
<td>OFF</td>
<td>ON</td>
<td>Data sent by the DTE is correctly received by the module. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. RTS line will be ON).</td>
</tr>
<tr>
<td>3</td>
<td>Enabled (AT&amp;K3)</td>
<td>OFF</td>
<td>OFF</td>
<td>Data sent by the DTE is buffered by the DTE and will be correctly received by the module when it is ready to receive data (when the UART is enabled). Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. RTS line will be ON).</td>
</tr>
<tr>
<td>3</td>
<td>Disabled (AT&amp;KO)</td>
<td>ON or OFF</td>
<td>ON</td>
<td>Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.</td>
</tr>
<tr>
<td>3</td>
<td>Disabled (AT&amp;KO)</td>
<td>ON or OFF</td>
<td>OFF</td>
<td>Data sent by the DTE is lost by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.</td>
</tr>
</tbody>
</table>

Table 12: UART and power-saving summary

**AT+UPSV=0: power saving disabled, fixed active-mode**

The module does not enter low power idle-mode and the UART interface is enabled (data can be sent and received): the CTS line is always held in the ON state after UART initialization. This is the default configuration.

**AT+UPSV=1: power saving enabled, cyclic idle/active-mode**

When the AT+UPSV=1 command is issued by the DTE, the UART is disabled after the timeout set by the second parameter of the +UPSV AT command (for more details see u-blox AT commands Manual [3]). Afterwards, the UART is enabled again, and the module does not enter low power idle-mode, as following:

- Periodically, for paging reception (see section 1.5.1.5) or other activities, to temporarily receive or send data over the UART, e.g. data buffered by the DTE with HW flow control enabled will be correctly received
- If the module needs to transmit some data (e.g. URC), the UART is temporarily enabled to send data
- If the DTE send data with HW flow control disabled, the first character sent causes the UART and module wake-up after ~5 ms: recognition of subsequent characters is guaranteed only after the complete wake-up (see the following subsection “wake up via data reception”)

The module automatically enters the low power idle-mode whenever possible but it wakes up to active-mode according to the UART periodic wake up so that the module cyclically enters the low power idle-mode and the active-mode. Additionally, the module wakes up to active-mode according to any required activity related to the network (e.g. for the periodic paging reception described in section 1.5.1.5, or for any other required RF Tx / Rx) or any other required activity related to module functions / interfaces (including the UART itself).

When the UART interface is enabled, data can be received. When a character is received, it forces the UART interface to stay enabled for a longer time and it forces the module to stay in the active-mode for a longer time, according to the timeout configured by the second parameter of the +UPSV AT command. The timeout can be set from 40 2G-frames (i.e. 40 x 4.615 ms = 184 ms) up to 65000 2G-frames (i.e. 65000 x 4.615 ms = 300 s). Default value is 2000 2G-frames (i.e. 2000 x 4.615 ms = 9.2 s). Every subsequent character received during the active-mode, resets and restarts the timer; hence the active-mode duration can be extended indefinitely.

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ubx

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The CTS output line is driven to the ON or OFF state when the module is either able or not able to accept data from the DTE over the UART: Figure 23 illustrates the CTS output line toggling due to paging reception and data received over the UART, with AT+UPSV=1 configuration.

![CTS output pin](image)

**Figure 23:** CTS output pin indicates when module’s UART is enabled (CTS = ON = low level) or disabled (CTS = OFF = high level)

**AT+UPSV=2: power saving enabled and controlled by the RTS line**

This configuration can only be enabled with the module hardware flow control disabled (i.e. AT&K0 setting). The UART interface is disabled after the DTE sets the RTS line to OFF. Afterwards, the UART is enabled again, and the module does not enter low power idle-mode, as following:

- If an OFF-to-ON transition occurs on the RTS input line, this causes the UART / module wake-up after ~5 ms: recognition of subsequent characters is guaranteed only after the complete wake-up, and the UART is kept enabled as long as the RTS input line is set to ON.
- If the module needs to transmit some data (e.g. URC), the UART is temporarily enabled to send data
- If the DTE sends data, the first character sent causes the wake-up of UART / module product versions “01”, “60” and TOBY-L201-02S after ~5 ms: recognition of subsequent characters is guaranteed only after the complete wake-up, and the UART will be then kept enabled after last data received according to the timeout previously set with AT+UPSV=1 configuration (see following subsection “wake up via data reception”)

The module automatically enters the low power idle-mode whenever possible but it wakes up to active-mode according to any required activity related to the network (e.g. for the periodic paging reception described in section 1.5.1.5, or for any other required RF transmission / reception) or any other required activity related to the module functions / interfaces (including the UART itself).

The hardware flow-control output (CTS line) indicates when the module is either able or not able to accept data from the DTE over the UART, even if hardware flow control is disabled with AT+UPSV=2 configuration.

**AT+UPSV=3: power saving enabled and controlled by the DTR line**

The UART interface is disabled after the DTE sets the DTR line to OFF. Afterwards, the UART is enabled again, and the module does not enter low power idle-mode, as following:

- If an OFF-to-ON transition occurs on the DTR input line, this causes the UART / module wake-up after ~5 ms: recognition of subsequent characters is guaranteed only after the complete wake-up, and the UART is kept enabled as long as the DTR input line is set to ON
- If the module needs to transmit some data (e.g. URC), the UART is temporarily enabled to send data
- If the DTE sends data, the first character sent causes the wake-up of UART / module product versions “01”, “60” and TOBY-L201-02S after ~5 ms: recognition of subsequent characters is guaranteed only after the complete wake-up, and the UART will be then kept enabled after last data received according to the timeout previously set with AT+UPSV=1 configuration (see following subsection “wake up via data reception”)

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The module automatically enters the low power idle-mode whenever possible but it wakes up to active-mode according to any required activity related to the network (e.g. for the periodic paging reception described in section 1.5.1.5, or for any other required RF signal transmission or reception) or any other required activity related to the functions/interfaces of the module.

The AT+UPSV=3 configuration can be enabled regardless the flow control setting on UART. In particular, the HW flow control can be enabled (AT&K3) or disabled (AT&K0) on UART during this configuration. In both cases, with the AT+UPSV=3 configuration, the CTS line indicates when the module is either able or not able to accept data from the DTE over the UART.

When the AT+UPSV=3 configuration is enabled, the DTR input line can still be used by the DTE to control the module behavior according to AT&D command configuration (see u-blox AT commands Manual [3]).

**Wake up via data reception**

The UART wake up via data reception consists of a special configuration of the module TXD input line that causes the system wake-up when a low-to-high transition occurs on the TXD input line. In particular, the UART is enabled and the module switches from the low power idle-mode to active-mode within ~5 ms from the first character received: this is the system “wake up time”.

As a consequence, the first character sent by the DTE when the UART is disabled (i.e. the wake up character) is not a valid communication character even if the wake up via data reception configuration is active, because it cannot be recognized, and the recognition of the subsequent characters is guaranteed only after the complete system wake-up (i.e. after ~5 ms).

The TXD input line is configured to wake up the system via data reception in the following case:

- AT+UPSV=1 is set with HW flow control disabled

The TXD input line on “01”, “60” and TOBY-L201-02S modules product versions is additionally configured to wake up the system via data reception in the following cases:

- AT+UPSV=2 is set with HW flow control disabled, and the RTS line is set OFF
- AT+UPSV=3 is set with HW flow control disabled, and the DTR line is set OFF

Figure 24 and Figure 25 show examples of common scenarios and timing constraints:

- AT+UPSV=1 power saving configuration is active and the timeout from last data received to idle-mode start is set to 2000 frames (AT+UPSV=1,2000)
- Hardware flow control is disabled

Figure 24 shows the case where the module UART is disabled and only a wake-up is forced. In this scenario the only character sent by the DTE is the wake-up character; as a consequence, the DCE module UART is disabled when the timeout from last data received expires (2000 frames without data reception, as the default case).

**Figure 24: Wake-up via data reception without further communication**

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Figure 25 shows the case where in addition to the wake-up character further (valid) characters are sent. The wake up character wakes-up the module UART. The other characters must be sent after the “wake up time” of ~5 ms. If this condition is satisfied, the module (DCE) recognizes characters. The module will disable the UART after 2000 GSM frames from the latest data reception.

![Diagram showing UART operation](image)

**Figure 25: Wake-up via data reception with further communication**

- The “wake-up via data reception” feature cannot be disabled.

  - In command mode\(^{17}\), with “wake-up via data reception” enabled and autobauding enabled, the DTE should always send a dummy character to the module before the “AT” prefix set at the beginning of each command line: the first dummy character is ignored if the module is in active-mode, or it represents the wake-up character if the module is in low power idle-mode.

  - In command mode\(^{17}\), with “wake-up via data reception” enabled and autobauding disabled, the DTE should always send a dummy “AT” to the module before each command line: the first dummy “AT” is not ignored if the module is in active-mode (i.e. the module replies “OK”), or it represents the wake up character if the module is in low power idle-mode (i.e. the module does not reply).

**Additional considerations**

If the USB is connected and not suspended, the module is forced to stay in active-mode, therefore the AT+UPSV settings are overruled but they have effect on the UART behavior (they configure UART power saving, so that UART is enabled / disabled according to the AT+UPSV settings).

#### 1.9.2.5 UART multiplexer protocol

TOBY-L2 series modules include multiplexer functionality as per 3GPP TS 27.010 [11], on the UART physical link. This is a data link protocol which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows a number of simultaneous sessions over the used physical link (UART): the user can concurrently use AT interface on one MUX channel and data communication on another MUX channel. The following virtual channels are defined (for more details, see Mux implementation Application Note [12]):

- Channel 0: control channel
- Channel 1 – 5: AT commands / data connection

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\(^{17}\) See the u-blox AT Commands Manual [3] for the definition of the interface data mode, command mode and online command mode.
1.9.3 DDC (I²C) interface

- The I²C bus compatible Display Data Channel interface is not available on the MPCI-L2 series modules.
- The I²C bus compatible Display Data Channel interface is not supported by the TOBY-L2 series modules “00”, “01”, “60” and TOBY-L201-02S product versions.

The SDA and SCL pins of TOBY-L2 series modules represent an I²C bus compatible Display Data Channel (DDC) interface for the communication with external I²C devices as audio codecs: an I²C master can communicate with more I²C slaves in accordance to the I²C bus specifications [13].

The AT commands interface is not available on the DDC (I²C) interface.

DDC (I²C) slave-mode operation is not supported: the TOBY-L2 series module can act as I²C master only.

The DDC (I²C) interface pads of the module, serial data (SDA) and serial clock (SCL), are open drain output and external pull up resistors must be used conforming to the I²C bus specifications [13].

1.9.4 Secure Digital Input Output interface (SDIO)

- Secure Digital Input Output interface is not available on MPCI-L2 series modules.
- Secure Digital Input Output interface is not supported by TOBY-L2 “00”, “01”, “60” product versions.

TOBY-L2 series modules include a 4-bit Secure Digital Input Output interface (SDIO_D0, SDIO_D1, SDIO_D2, SDIO_D3, SDIO_CLK, SDIO_CMD) designed to communicate with an external u-blox short range Wi-Fi module: the TOBY-L2 cellular module acts as an SDIO host controller which can communicate over the SDIO bus with a compatible u-blox short range Wi-Fi module acting as SDIO device.

The SDIO interface is the only one interface of TOBY-L2 series modules dedicated for communication between the u-blox cellular module and the u-blox short range Wi-Fi module. The AT commands interface is not available on the SDIO interface of TOBY-L2 series modules.

The SDIO interface supports 50 MHz bus clock frequency, which allows a data throughput of 200 Mb/s.

Combining a u-blox cellular module with a u-blox short range communication module gives designers full access to the Wi-Fi module directly via the cellular module, so that a second interface connected to the Wi-Fi module is not necessary. AT commands via the AT interfaces of the cellular module (UART, USB) allows a full control of the Wi-Fi module from any host processor, because Wi-Fi control messages are relayed to the Wi-Fi module via the dedicated SDIO interface (for more details, see the Wi-Fi AT commands in the u-blox AT Commands Manual [3]).

u-blox has implemented special features in the cellular modules to ease the design effort for the integration of a u-blox cellular module with a u-blox short range Wi-Fi module to provide Router functionality (for more details, see the Wi-Fi / Cellular Integration Application Note [15]).

Additional custom function over GPIO pins is designed to improve the integration with u-blox Wi-Fi modules:

- Wi-Fi enable Switch-on / switch-off the Wi-Fi

- GPIOs are not supported by TOBY-L2 “00”, “01” and “60” product versions, except for the Wireless Wide Area Network status indication configured on GPIO1 pin.
- GPIOs are not available on MPCI-L2 series modules.
1.10 Audio

1.10.1 Digital audio over I²S interface

- I²S digital audio interface is not available on MPCI-L2 modules.

TOBY-L2 series modules include a 4-wire I²S digital audio interface (I2S_TXD data output, I2S_RXD data input, I2S_CLK clock output, I2S_WA world alignment / synchronization signal output) that can be configured by AT command for digital audio communication with external digital audio devices as an audio codec (for more details see the u-blox AT Commands Manual [3], +UI2S AT command).

The I²S interface can be set to two modes, by the <I2S_mode> parameter of the AT+UI2S command:

- PCM mode (short synchronization signal): I²S word alignment signal is set high for 1 or 2 clock cycles for the synchronization, and then is set low for 31 or 30 clock cycles according to the 32 clock cycles frame length.
- Normal I²S mode (long synchronization signal): I²S word alignment is set high / low with a 50% duty cycle (high for 16 clock cycles / low for 16 clock cycles, according to the 32 clock cycles frame length).

The modules support I²S master role only: I2S_CLK clock and I2S_WA world alignment / synchronization signal are generated by the module.

The sample rate of transmitted/received words, which corresponds to the I²S word alignment / synchronization signal frequency, can be set by the <I2S_sample_rate> parameter of AT+UI2S to:

- 8 kHz
- 16 kHz

The modules support I²S transmit and I²S receive data 16-bit words long, linear, mono. Data is transmitted and read in 2’s complement notation. MSB is transmitted and read first.

I²S clock signal frequency is set to 32 x <I2S_sample_rate>: the frame length, which corresponds to the I²S word alignment / synchronization signal period, is 32 I²S clock cycles long.

For the complete description of the possible configurations and settings of the I²S digital audio interface for PCM and Normal I²S modes refer to the u-blox AT Commands Manual [3], +UI2S AT command.

The internal audio processing system is summarized in Figure 26: external digital audio devices can be interfaced directly to the digital signal processing part via the I²S digital interface. Audio processing can be controlled by AT commands: see Audio Interface and Audio Parameters Tuning sections in the u-blox AT Commands Manual [3].

Figure 26: TOBY-L2 modules internal audio processing system block diagram

The internal audio processing system of TOBY-L2 modules does not support the side-tone.
1.11 General Purpose Input/Output

GPIOs are not supported by TOBY-L2 modules “00”, “01” and “60” product versions, except for the Wireless Wide Area Network status indication configured on GPIO1 pin.

- GPIOs are not available on MPCI-L2 series modules.

TOBY-L2 series modules include 14 pins (GPIO1-GPIO6, I2S_TXD, I2S_RXD, I2S_CLK, I2S_WA, DTR, DSR, DCD, RI) that can be configured as General Purpose Input/Output or to provide custom functions via u-blox AT commands (see the u-blox AT Commands Manual [3], +UGPIOC, +UGPIOR, +UGPIOW AT commands), as summarized in Table 13.

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
<th>Default GPIO</th>
<th>Configurable GPIOs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Network status indication</td>
<td>Network status: registered home network, registered roaming, data transmission, no service</td>
<td>--</td>
<td>All</td>
</tr>
<tr>
<td>SIM card detection</td>
<td>SIM card physical presence detection</td>
<td>GPIO5</td>
<td>GPIO5</td>
</tr>
<tr>
<td>SIM card hot insertion/removal</td>
<td>Enable / disable SIM interface upon detection of external SIM card physical insertion / removal</td>
<td>--</td>
<td>GPIO5</td>
</tr>
<tr>
<td>I2S digital audio interface</td>
<td>I2S digital audio interface</td>
<td>I2S_RXD, I2S_TXD, I2S_CLK, I2S_WA</td>
<td>I2S_RXD, I2S_TXD, I2S_CLK, I2S_WA</td>
</tr>
<tr>
<td>Master clock output²</td>
<td>13 MHz / 26 MHz clock output for an external device as an audio codec</td>
<td>GPIO6</td>
<td>GPIO6</td>
</tr>
<tr>
<td>Wi-Fi enable</td>
<td>Enable/disable the supply of the external u-blox Wi-Fi module connected to the cellular module</td>
<td>GPIO1</td>
<td>All</td>
</tr>
<tr>
<td>DSR</td>
<td>UART data set ready output</td>
<td>DSR</td>
<td>DSR</td>
</tr>
<tr>
<td>DTR</td>
<td>UART data terminal ready input</td>
<td>DTR</td>
<td>DTR</td>
</tr>
<tr>
<td>DCD</td>
<td>UART data carrier detect output</td>
<td>DCD</td>
<td>DCD</td>
</tr>
<tr>
<td>RI</td>
<td>UART ring indicator output</td>
<td>RI</td>
<td>RI</td>
</tr>
<tr>
<td>General purpose input</td>
<td>Input to sense high or low digital level</td>
<td>--</td>
<td>All</td>
</tr>
<tr>
<td>General purpose output</td>
<td>Output to set the high or the low digital level</td>
<td>GPIO4</td>
<td>All</td>
</tr>
<tr>
<td>Pin disabled</td>
<td>Tri-state with an internal active pull-down enabled</td>
<td>GPIO2, GPIO3</td>
<td>All</td>
</tr>
</tbody>
</table>

Table 13: TOBY-L2 series GPIO custom functions configuration

² Not supported by TOBY-L201-02S and TOBY-L220-62S product versions.
1.12 Mini PCIe specific signals (W_DISABLE#, LED_WWAN#)

Mini PCI Express specific signals (W_DISABLE#, LED_WWAN#) are not available on TOBY-L2 series.

MPCI-L2 series modules include the W_DISABLE# active-low input signal to disable the radio operations as specified by the PCI Express Mini Card Electromechanical Specification [16].

As described in Figure 27, the W_DISABLE# input is equipped with an internal pull-up to the 3.3Vaux supply. The W_DISABLE# input detailed electrical characteristics are described in the MPCI-L2 series Data Sheet [2].

![Figure 27: MPCI-L2 series modules W_DISABLE# input circuit description](image)

MPCI-L2 series modules include the LED_WWAN# active-low open drain output to provide the Wireless Wide Area Network status indication as specified by the PCI Express Mini Card Electromechanical Specification [16].

For more electrical characteristics details see the MPCI-L2 Data Sheet [2].

1.13 Reserved pins (RSVD)

Pins reserved for future use, marked as RSVD, are not available on MPCI-L2 series.

TOBY-L2 series modules have pins reserved for future use, marked as RSVD: they can all be left unconnected on the application board, except the RSVD pin number 6 that must be externally connected to ground.

1.14 Not connected pins (NC)

Pins internally not connected, marked as NC, are not available on TOBY-L2 series.

MPCI-L2 series modules have pins internally not connected, marked as NC: they can be left unconnected or they can be connected on the application board according to any application requirement, given that none function is provided by the modules over these pins.
1.15 System features

1.15.1 Network indication

- MPCI-L2 series modules include the LED_WWAN# active-low open drain output to provide the Wireless Wide Area Network status indication as per PCI Express Mini Card Electromechanical Specification [16].
- GPIOs are not supported by TOBY-L2 modules “00”, “01”, “60” product versions, but the Wireless Wide Area Network status indication is by default configured on the GPIO1 pin.

The GPIO1 can be configured by the AT+UGPIOC command (for further details see the u-blox AT Commands Manual [3]), to indicate network status as described below:
- No service (no network coverage or not registered)
- Registered 2G / 3G / LTE home network
- Registered 2G / 3G / LTE visitor network (roaming)
- Call enabled (RF data transmission / reception)

1.15.2 Antenna supervisor

- Antenna supervisor (i.e. antenna detection) is not available on MPCI-L2 series.
- Antenna supervisor (i.e. antenna detection) is not supported by TOBY-L2 series modules “00”, “01” and “60” product versions.

The antenna detection function provided by the ANT_DET pin is based on an ADC measurement as optional feature that can be implemented if the application requires it. The antenna supervisor is forced by the +UANTR AT command (see the u-blox AT Commands Manual [3] for more details).

The requirements to achieve antenna detection functionality are the following:
- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 1.7.2 for detailed antenna detection interface functional description and see section 2.4.2 for detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

1.15.3 Jamming detection

- Congestion detection (i.e. jamming detection) is not supported by “00”, “01”, “02” “03”, “60” and “62” product versions.

In real network situations modules can experience various kind of out-of-coverage conditions: limited service conditions when roaming to networks not supporting the specific SIM, limited service in cells which are not suitable or barred due to operators’ choices, no cell condition when moving to poorly served or highly interfered areas. In the latter case, interference can be artificially injected in the environment by a noise generator covering a given spectrum, thus obscuring the operator's carriers entitled to give access to the LTE/3G/2G service.

The congestion (i.e. jamming) detection feature can be enabled and configured by the +UCD AT command: the feature consists of detecting an anomalous source of interference and signaling the start and stop of such conditions to the host application processor with an unsolicited indication, which can react appropriately by e.g. switching off the radio transceiver of the module (i.e. configuring the module in “airplane mode” by means of the +CFUN AT command) in order to reduce power consumption and monitoring the environment at constant periods (for more details see the u-blox AT Commands Manual [3]).
**1.15.4 IP modes of operation**

IP modes of operation refer to the TOBY-L2 and MPCI-L2 series modules configuration related to the network IP termination and network interfaces settings in general. IP modes of operation are the following:

- **Bridge mode:** In bridge mode the module acts as a cellular modem dongle connected to the host over serial interface. The IP termination of the network is placed on the host IP stack. The module is configured as a bridge which means the network IP address is assigned to the host (host IP termination).

- **Router mode:** In router mode the module acts as a cellular modem router which means the IP termination of the network is placed on the internal IP stack of the module (on-target IP termination). In particular, in this configuration the application processor belongs to a private network and is not aware of the mobile connectivity setup of the module.

For more details about IP modes of operation see the u-blox AT Commands Manual [3].

**1.15.5 Dual stack IPv4/IPv6**

TOBY-L2 and MPCI-L2 series support both Internet Protocol version 4 and Internet Protocol version 6 in parallel. For more details about dual stack IPv4/IPv6 see the u-blox AT Commands Manual [3].

**1.15.6 TCP/IP and UDP/IP**

Embeded TCP/IP and UDP/IP stack as well as Direct Link mode are not supported by the “00” and “60” product versions.

TOBY-L2 and MPCI-L2 series modules provide embedded TCP/IP and UDP/IP protocol stack: a PDP context can be configured, established and handled via the data connection management packet switched data commands.

TOBY-L2 and MPCI-L2 series modules provide Direct Link mode to establish a transparent end-to-end communication with an already connected TCP or UDP socket via serial interfaces (USB, UART). In Direct Link mode, data sent to the serial interface from an external application processor is forwarded to the network and vice-versa.

For more details about embedded TCP/IP and UDP/IP functionalities see the u-blox AT Commands Manual [3].

**1.15.7 FTP**

Embeded FTP services as well as Direct Link mode are not supported by “00” and “60” product versions.

TOBY-L2 and MPCI-L2 series provide embedded File Transfer Protocol (FTP) services. Files are read and stored in the local file system of the module.

FTP files can also be transferred using FTP Direct Link:

- **FTP download:** data coming from the FTP server is forwarded to the host processor via USB / UART serial interfaces (for FTP without Direct Link mode the data is always stored in the module’s Flash File System)

- **FTP upload:** data coming from the host processor via USB / UART serial interface is forwarded to the FTP server (for FTP without Direct Link mode the data is read from the module’s Flash File System)

When Direct Link is used for a FTP file transfer, only the file content pass through USB / UART serial interface, whereas all the FTP commands handling is managed internally by the FTP application.

For more details about embedded FTP functionalities see u-blox AT Commands Manual [3].
1.15.8 HTTP

Embedded HTTP services are not supported by “00” and “60” product versions.

TOBY-L2 and MPCI-L2 series modules provide the embedded Hyper-Text Transfer Protocol (HTTP) services via AT commands for sending requests to a remote HTTP server, receiving the server response and transparently storing it in the module’s Flash File System (FFS).

For more details about embedded HTTP functionalities see the u-blox AT Commands Manual [3].

1.15.9 SSL / TLS

Embedded Secure Sockets Layer (SSL) / Transport Layer Security (TLS) protocols are not supported by the “00”, “01”, “60”, TOBY-L201-02S and MPCI-L201-02S product versions.

TOBY-L2 and MPCI-L2 series modules support the Secure Sockets Layer (SSL) / Transport Layer Security (TLS) with certificate key sizes up to 4096 bits to provide security over the FTP and HTTP protocols.

The SSL/TLS support provides different connection security aspects:

- Server authentication: use of the server certificate verification against a specific trusted certificate or a trusted certificates list
- Client authentication: use of the client certificate and the corresponding private key
- Data security and integrity: data encryption and Hash Message Authentication Code (HMAC) generation

The security aspects used during a connection depend on the SSL/TLS configuration and features supported. Table 14 contains the settings of the default SSL/TLS profile and Table 15 to Table 19 report the main SSL/TLS supported capabilities of the products. For a complete list of supported configurations and settings see the u-blox AT Commands Manual [3].

<table>
<thead>
<tr>
<th>Settings</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Certificates validation level</td>
<td>Level 0</td>
<td>The server certificate will not be checked or verified</td>
</tr>
<tr>
<td>Minimum SSL/TLS version</td>
<td>Any</td>
<td>The server can use any of the TLS1.0/TLS1.1/TLS1.2 versions for the connection</td>
</tr>
<tr>
<td>Cipher suite</td>
<td>Automatic</td>
<td>The cipher suite will be negotiated in the handshake process</td>
</tr>
<tr>
<td>Trusted root certificate internal name</td>
<td>None</td>
<td>No certificate will be used for the server authentication</td>
</tr>
<tr>
<td>Expected server host-name</td>
<td>None</td>
<td>No server host-name is expected</td>
</tr>
<tr>
<td>Client certificate internal name</td>
<td>None</td>
<td>No client certificate will be used</td>
</tr>
<tr>
<td>Client private key internal name</td>
<td>None</td>
<td>No client private key will be used</td>
</tr>
<tr>
<td>Client private key password</td>
<td>None</td>
<td>No client private key password will be used</td>
</tr>
<tr>
<td>Pre-shared key</td>
<td>None</td>
<td>No pre-shared key password will be used</td>
</tr>
</tbody>
</table>

Table 14: Default SSL/TLS profile

<table>
<thead>
<tr>
<th>SSL/TLS Version</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSL 2.0</td>
<td>NO</td>
</tr>
<tr>
<td>SSL 3.0</td>
<td>YES</td>
</tr>
<tr>
<td>TLS 1.0</td>
<td>YES</td>
</tr>
<tr>
<td>TLS 1.1</td>
<td>YES</td>
</tr>
<tr>
<td>TLS 1.2</td>
<td>YES</td>
</tr>
</tbody>
</table>

Table 15: SSL/TLS version support
1.15.10 Bearer Independent Protocol

BIP is not supported by the “00”, “60” product versions.

The Bearer Independent Protocol (BIP) is a mechanism by which a cellular module provides a SIM with access to the data bearers supported by the network. With the BIP for Over-the-Air SIM provisioning, the data transfer from and to the SIM uses either an already active PDP context or a new PDP context established with the APN provided by the SIM card. For more details, see the u-blox AT Commands Manual [3].
1.15.11 Wi-Fi integration

- u-blox short range communication Wi-Fi modules integration is not available for MPCI-L2 series modules.
- u-blox short range communication Wi-Fi modules integration is not supported by the TOBY-L2 series modules “00”, “01” and “60” product versions.

Full access to u-blox short range communication Wi-Fi modules is available through a dedicated SDIO interface (see sections 1.9.4 and 2.6.4). This means that combining a TOBY-L2 series cellular module with a u-blox short range communication module gives designers full access to the Wi-Fi module directly via the cellular module, so that a second interface connected to the Wi-Fi module is not necessary.

AT commands via the AT interfaces of the cellular module (UART, USB) allows a full control of the Wi-Fi module from any host processor, because Wi-Fi control messages are relayed to the Wi-Fi module via the dedicated SDIO interface (for more details, see the Wi-Fi AT commands in the u-blox AT Commands Manual [3]).

All the management software for Wi-Fi module operations runs inside the cellular module in addition to those required for cellular-only operation: Wi-Fi driver, Web User Interface (WebUI), Connection Config Manager.

For more details, see the Wi-Fi / Cellular Integration Application Note [15].

1.15.12 Firmware update Over AT (FOAT)

This feature allows upgrading the module firmware over USB / UART serial interfaces, using AT commands.

- The +UFWUPD AT command triggers a reboot followed by the upgrade procedure at specified a baud rate
- A special boot loader on the module performs firmware installation, security verifications and module reboot
- Firmware authenticity verification is performed via a security signature during the download. The firmware is then installed, overwriting the current version. In case of power loss during this phase, the boot loader detects a fault at the next wake-up, and restarts the firmware download. After completing the upgrade, the module is reset again and wakes-up in normal boot

For more details about Firmware update Over AT procedure see the Firmware Update Application Note [6] and the u-blox AT Commands Manual [3], +UFWUPD AT command.

1.15.13 Firmware update Over The Air (FOTA)

Firmware update Over The Air (FOTA) is not supported by “00” and “60” product versions.

This feature allows upgrading the module firmware over the LTE/3G/2G air interface.

In order to reduce the amount of data to be transmitted over the air, the implemented FOTA feature requires downloading only a “delta file” instead of the full firmware. The delta file contains only the differences between the two firmware versions (old and new), and is compressed. The firmware update procedure can be triggered using dedicated AT command with the delta file stored in the module file system via over the air FTP.

For more details about Firmware update Over The Air procedure see the Firmware Update Application Note [6] and the u-blox AT Commands Manual [3], +UFWINSTALL AT command.
1.15.14 Smart temperature management

Smart temperature management is not supported by “00”, “01” and “60” product versions.

Cellular modules – independent of the specific model – always have a well defined operating temperature range. This range should be respected to guarantee full device functionality and long life span.

Nevertheless there are environmental conditions that can affect operating temperature, e.g. if the device is located near a heating/cooling source, if there is/isn’t air circulating, etc.

The module itself can also influence the environmental conditions; such as when it is transmitting at full power. In this case its temperature increases very quickly and can raise the temperature nearby.

The best solution is always to properly design the system where the module is integrated. Nevertheless an extra check/security mechanism embedded into the module is a good solution to prevent operation of the device outside of the specified range.

Smart Temperature Supervisor (STS)

The Smart Temperature Supervisor is activated and configured by a dedicated AT+USTS command. See the u-blox AT Commands Manual [3] for more details.

The cellular module measures the internal temperature (Ti) and its value is compared with predefined thresholds to identify the actual working temperature range.

Temperature measurement is done inside the cellular module: the measured value could be different from the environmental temperature (Ta).

Temperature range and limits

The entire temperature range is divided into sub-regions by limits (see Figure 28) named t-2, t-1, t+1, and t+2.

- Within the first limit, (t-1 < Ti < t+1), the cellular module is in the normal working range, the Safe Area
- In the Warning Area, (t-2 < Ti < t-1) or (t+1 < Ti < t+2), the cellular module is still inside the valid temperature range, but the measured temperature approaches the limit (upper or lower). The module sends a warning to the user (through the active AT communication interface), which can take, if possible, the necessary actions to return to a safer temperature range or simply ignore the indication. The module is still in a valid and good working condition
- Outside the valid temperature range, (Ti < t-2) or (Ti > t+2), the device is working outside the specified range and represents a dangerous working condition. This condition is indicated and the device shuts down to avoid damage

For security reasons the shutdown is suspended in case an emergency call in progress. In this case the device will switch off at call termination.

The user can decide at anytime to enable/disable the Smart Temperature Supervisor feature. If the feature is disabled there is no embedded protection against disallowed temperature conditions.
Figure 29 shows the flow diagram implemented for the Smart Temperature Supervisor.

Feature enabled (full logic or indication only)

Feature disabled: no action

Temperature is within normal operating range

Temperature is outside valid temperature range

Tempertature is back to safe area

Send notification (safe)

Send notification (warning)

Send notification (dangerous)

Wait emergency call termination

Yes

No

Yes

No

Yes

No

Yes

No

Yes

No

Yes

No

Send shutdown notification

Shut the device down

Figure 29: Smart Temperature Supervisor (STS) flow diagram
Threshold Definitions

When the application of cellular module operates at extreme temperatures with Smart Temperature Supervisor enabled, the user should note that outside the valid temperature range the device will automatically shut down as described above.

The input for the algorithm is always the temperature measured within the cellular module \( (T_i, \text{internal}) \). This value can be higher than the working ambient temperature \( (T_a, \text{ambient}) \), as (for example) during transmission at maximum power a significant fraction of DC input power is dissipated as heat. This behavior is partially compensated by the definition of the upper shutdown threshold \( (t_{+\text{-}2}) \) that is slightly higher than the declared environmental temperature limit.

The temperature thresholds are defined according the Table 20.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Temperature</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{-2} )</td>
<td>Low temperature shutdown</td>
<td>-40 °C</td>
<td>Equal to the absolute minimum temperature rating for the wireless module (the lower limit of the extended temperature range)</td>
</tr>
<tr>
<td>( t_{-1} )</td>
<td>Low temperature warning</td>
<td>-30 °C</td>
<td>10°C above ( t_{-2} )</td>
</tr>
<tr>
<td>( t_{+1} )</td>
<td>High temperature warning</td>
<td>+77 °C</td>
<td>20°C below ( t_{+2} ). The higher warning area for upper range ensures that any countermeasures used to limit the thermal heating will become effective, even considering some thermal inertia of the complete assembly.</td>
</tr>
<tr>
<td>( t_{+2} )</td>
<td>High temperature shutdown</td>
<td>+97 °C</td>
<td>Equal to the internal temperature ( T_i ) measured in the worst case operating condition at typical supply voltage when the ambient temperature ( T_a ) in the reference setup. ** equals the absolute maximum temperature rating (upper limit of the extended temperature range)</td>
</tr>
</tbody>
</table>

* +90 °C for TOBY-L201-02S and MPCI-L201-02S product versions

** Module mounted on a 79 mm x 62 mm x 1.46 mm 4-Layers PCB with a high coverage of copper within climatic chamber

Table 20: Thresholds definition for Smart Temperature Supervisor

The sensor measures board temperature inside the shields, which can differ from ambient temperature.

1.15.15 SIM Access Profile (SAP)

SIM access profile (SAP) feature allows cellular modules to access and use a remote (U)SIM card instead of the local SIM card directly connected to the module (U)SIM interface.

The modules provide a dedicated USB SAP channel for communication with the remote (U)SIM card.

The communication between u-blox cellular modules and the remote SIM is conformed to client-server paradigm: the module is the SAP client establishing a connection and performing data exchange to an SAP server directly connected to the remote SIM that is used by the module for cellular network operations. The SAP communication protocol is based on the SIM Access Profile Interoperability Specification [29].

u-blox cellular modules do not support SAP server role: the module acts as SAP client only.

A typical application using the SAP feature is the scenario where a device such as an embedded car-phone with an integrated TOBY-L2 module uses a remote SIM included in an external user device (e.g. a simple SIM card reader or a portable phone), which is brought into the car. The car-phone accesses the cellular network using the remote SIM in the external device.

u-blox cellular modules, acting as an SAP client, can be connected to an SAP server by a completely wired connection, as shown in Figure 30.
As stated in the SIM Access Profile Interoperability Specification [29], the SAP client can be connected to the SAP server by means of a Bluetooth wireless link, using additional Bluetooth transceivers. In this case, the application processor wired to TOBY-L2 modules establishes and controls the Bluetooth connection using the SAP profile, and routes data received over a serial interface channel to data transferred over a Bluetooth interface and vice versa, as shown in Figure 31.

The application processor can start an SAP connection negotiation between TOBY-L2 module SAP client and an SAP server using a custom AT command (for more details see the u-blox AT Commands Manual [3]).

While the connection with the SAP server is not fully established, the TOBY-L2 module continues to operate with the attached (local) SIM, if present. Once the connection is established and negotiated, the module performs a detach operation from the local SIM followed by an attach operation to the remote one. Then the remotely attached SIM is used for any cellular network operation.

URC indications are provided to inform the user about the state of both the local and remote SIM. The insertion and the removal of the local SIM card are notified if a proper card presence detection circuit using the SIM_DET pin of TOBY-L2 modules is implemented as shown in the section 2.5, and if the related “SIM card detection” and “SIM hot insertion/removal” functions are enabled by AT commands (for more details see u-blox AT Commands Manual [3], +UGPIOC, +UDCONF=50 AT commands).

Upon SAP deactivation, the TOBY-L2 modules perform a detach operation from the remote SIM followed by an attach operation to the local one, if present.
1.15.16 Power saving

The power saving configuration is by default disabled, but it can be enabled using the AT+UPSV command (for the complete description of the AT+UPSV command, see the u-blox AT Commands Manual [3]). When power saving is enabled, the module automatically enters the low power idle-mode whenever possible, reducing current consumption (see section 1.5.1.5, TOBY-L2 Data Sheet [1] and MPCI-L2 Data Sheet [2]).

During the low power idle-mode, the module is not ready to communicate with an external device, as it is configured to reduce power consumption. The module wakes up from low power idle-mode to active-mode in the following events:

- Automatic periodic monitoring of the paging channel for the reception of the paging block sent by the base station according to network conditions (see section 1.5.1.5)
- The connected USB host forces a remote wakeup of the module as USB device (see section 1.9.1.4)
- Automatic periodic enable of the UART interface to receive / send data, with AT+UPSV=1 (see 1.9.2.4)
- Data received on UART interface, with HW flow control disabled and power saving enabled (see 1.9.2.4)
- **RTS** input set ON by the host DTE, with HW flow control disabled and AT+UPSV=2 (see 1.9.2.4)
- **DTR** input set ON by the host DTE, with AT+UPSV=3 (see 1.9.2.4)
- The connected SDIO device forces a wakeup of the module as SDIO host (see 1.9.4)
- A preset RTC alarm occurs (see u-blox AT Commands Manual [3], AT+CALA)

For the definition and the description of TOBY-L2 and MPCI-L2 series modules operating modes, including the events forcing transitions between the different operating modes, see the section 1.4.
2 Design-in

2.1 Overview

For an optimal integration of TOBY-L2 and MPCI-L2 series modules in the final application board follow the design guidelines stated in this section.

Every application circuit must be properly designed to guarantee the correct functionality of the relative interface, however a number of points require high attention during the design of the application device.

The following list provides a rank of importance in the application design, starting from the highest relevance:

1. Module antenna connection: **ANT1, ANT2** and **ANT_DET**.
   Antenna circuit directly affects the RF compliance of the device integrating a TOBY-L2 and MPCI-L2 series module with applicable certification schemes. Very carefully follow the suggestions provided in the relative section 2.4 for schematic and layout design.

2. Module supply: **VCC** or **3.3Vaux** and **GND** pins.
   The supply circuit affects the RF compliance of the device integrating a TOBY-L2 and MPCI-L2 series module with applicable required certification schemes as well as antenna circuit design. Very carefully follow the suggestions provided in the relative section 2.2.1 for schematic and layout design.

3. USB interface: **USB_D+, USB_D-** pins.
   Accurate design is required to guarantee USB 2.0 high-speed interface functionality. Carefully follow the suggestions provided in the relative section 2.6.1 for schematic and layout design.

4. SIM interface: **VSIM, SIM_CLK, SIM_IO, SIM_RST** or **UIM_PWR, UIM_DATA, UIM_CLK, UIM_RESET** pins.
   Accurate design is required to guarantee SIM card functionality reducing the risk of RF coupling. Carefully follow the suggestions provided in the relative section 2.5 for schematic and layout design.

5. SDIO interface: **SDIO_D0, SDIO_D1, SDIO_D2, SDIO_D3, SDIO_CLK, SDIO_CMD** pins.
   Accurate design is required to guarantee SDIO interface functionality. Carefully follow the suggestions provided in the relative section 2.6.4 for schematic and layout design.

6. System functions: **RESET_N** or **PERST#, PWR_ON** pins.
   Accurate design is required to guarantee that the voltage level is well defined during operation. Carefully follow the suggestions provided in the relative section 2.3 for schematic and layout design.

7. Other supplies: **V_BCKP** RTC supply and **V_INT** generic digital interfaces supply.
   Accurate design is required to guarantee proper functionality. Follow the suggestions provided in the corresponding sections 2.2.2 and 2.2.3 for schematic and layout design.

8. Other digital interfaces: UART, **I²C, I²S**, Host Select, GPIOs, Mini PCIe specific signals and Reserved pins.
   Accurate design is required to guarantee proper functionality. Follow the suggestions provided in sections 2.6.2, 2.6.3, 2.7.1, 2.3.3, 2.8, 2.9 and 2.10 for schematic and layout design.
2.2 Supply interfaces

2.2.1 Module supply (VCC or 3.3Vaux)

2.2.1.1 General guidelines for VCC or 3.3Vaux supply circuit selection and design

VCC or 3.3Vaux pins are internally connected. Application design shall connect all the available pads to the external supply to minimize the power loss due to series resistance.

GND pins are internally connected. Application design shall connect all the available pads to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

TOBY-L2 and MPCI-L2 series modules must be sourced through the VCC or the 3.3Vaux pins with a proper DC power supply that should meet the following prerequisites to comply with the modules’ VCC or 3.3Vaux requirements summarized in Table 7.

The proper DC power supply can be selected according to the application requirements (see Figure 32) between the different possible supply sources types, which most common ones are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery, for TOBY-L2 series only
- Primary (disposable) battery, for TOBY-L2 series only

![Figure 32: VCC supply concept selection](image_url)

The switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the operating supply voltage of TOBY-L2 and MPCI-L2 series. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See 2.2.1.2, 2.2.1.6, 2.2.1.9, 2.2.1.10 for specific design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less or equal than 5 V). In this case the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See 2.2.1.3, 2.2.1.6, 2.2.1.9, 2.2.1.10 for specific design-in.

If TOBY-L2 modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide VCC. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to VCC is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for VCC, and should therefore be avoided. See 2.2.1.4, 2.2.1.6, 2.2.1.9, 2.2.1.10 for specific design-in.

Keep in mind that the use of rechargeable batteries requires the implementation of a suitable charger circuit which is not included in the modules. The charger circuit has to be designed to prevent over-voltage on VCC pins of the module, and it should be selected according to the application requirements: a DC/DC switching
charger is the typical choice when the charging source has an high nominal voltage (e.g. ~12 V), whereas a linear charger is the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time in the application as possible supply source, then a proper charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery. See 2.2.1.7, 2.2.1.8 and 2.2.1.6, 2.2.1.9, 2.2.1.10 for specific design-in.

The use of a primary (not rechargeable) battery is in general uncommon, but appropriate parts can be selected given that the most cells available are seldom capable of delivering the maximum current specified in TOBY-L2 series Data Sheet [1] during connected-mode. Carefully evaluate the usage of super-capacitors as supply source since aging and temperature conditions significantly affect the actual capacitor characteristics. See 2.2.1.5 and 2.2.1.6, 2.2.1.9, 2.2.1.10 for specific design-in.

Rechargeable 3-cell Li-Ion or Li-Pol and Ni-MH chemistry batteries reach a maximum voltage that is above the maximum rating for the 3.3Vaux supply of MPCI-L2 modules, and should therefore be avoided. The use of rechargeable, not-rechargeable battery or super-capacitors is very uncommon for Mini PCI Express applications, so that these supply sources types are not considered for MPCI-L2 modules.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module VCC requirements summarized in Table 7.

### 2.2.1.2 Guidelines for VCC or 3.3Vaux supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail to the VCC or the 3.3Vaux value is high, since switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the VCC supply or the typical 3.3 V value of the 3.3Vaux supply.

The characteristics of the switching regulator connected to VCC or 3.3Vaux pins should meet the following prerequisites to comply with the module VCC or 3.3Vaux requirements summarized in Table 7:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the VCC or 3.3Vaux pins within the specified operating range and must be capable of delivering to VCC or 3.3Vaux pins the maximum peak / pulse current consumption during Tx burst at maximum Tx power specified in the TOBY-L2 series Data Sheet [1] or in the MPCI-L2 series Data Sheet [2].

- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) VCC or 3.3Vaux voltage profile.

- **High switching frequency**: for best performance and for smaller applications it is recommended to select a switching frequency ≥ 600 kHz (since L-C output filter is typically smaller for high switching frequency). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be carefully evaluated since this can produce noise in the VCC or 3.3Vaux voltage profile and therefore negatively impact LTE/3G/2G modulation spectrum performance. An additional L-C low-pass filter between the switching regulator output to VCC or 3.3Vaux supply pins can mitigate the ripple at the input of the module, but adds extra voltage drop due to resistive losses on series inductors.

- **PWM mode operation**: it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected-mode, the Pulse Frequency Modulation (PFM) mode and PFM/PWM modes transitions must be avoided to reduce the noise on the VCC or 3.3Vaux voltage profile. Switching regulators can be used that are able to switch between low ripple PWM mode and high ripple PFM mode, provided that the mode transition occurs when the module changes status from the idle/active-modes to connected-mode. It is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold.

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Design-in

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Figure 33 and Table 21 show an example of a high reliability power supply circuit, where the module VCC or 3.3Vaux input is supplied by a step-down switching regulator capable of delivering maximum current with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

![Circuit Diagram]

**Figure 33: Example of high reliability VCC and 3.3Vaux supply application circuit using a step-down regulator**

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>10 µF Capacitor Ceramic X7R 5750 15% 50 V</td>
<td>C5750X7R1H106MB - TDK</td>
</tr>
<tr>
<td>C2</td>
<td>10 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R71C103KA01 - Murata</td>
</tr>
<tr>
<td>C3</td>
<td>680 pF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R71H681KA01 - Murata</td>
</tr>
<tr>
<td>C4</td>
<td>22 pF Capacitor Ceramic C0G 0402 5% 25 V</td>
<td>GRM1555C1H220JZ01 - Murata</td>
</tr>
<tr>
<td>C5</td>
<td>10 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R71C103KA01 - Murata</td>
</tr>
<tr>
<td>C6</td>
<td>470 nF Capacitor Ceramic X7R 0603 10% 25 V</td>
<td>GRM188R71E474KA12 - Murata</td>
</tr>
<tr>
<td>C7</td>
<td>22 µF Capacitor Ceramic X5R 1210 10% 25 V</td>
<td>GRM32ER61E226KE15 - Murata</td>
</tr>
<tr>
<td>C8</td>
<td>330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ</td>
<td>T520D337M006ATE045 - KEMET</td>
</tr>
<tr>
<td>D1</td>
<td>Schottky Diode 40 V 3 A</td>
<td>MBRA340T3G - ON Semiconductor</td>
</tr>
<tr>
<td>L1</td>
<td>10 µH Inductor 744066100 30% 3.6 A</td>
<td>744066100 - Wurth Electronics</td>
</tr>
<tr>
<td>R1</td>
<td>470 kΩ Resistor 0402 5% 0.1 W</td>
<td>2322-705-87474-L - Yageo</td>
</tr>
<tr>
<td>R2</td>
<td>15 kΩ Resistor 0402 5% 0.1 W</td>
<td>2322-705-87153-L - Yageo</td>
</tr>
<tr>
<td>R3</td>
<td>22 kΩ Resistor 0402 5% 0.1 W</td>
<td>2322-705-87223-L - Yageo</td>
</tr>
<tr>
<td>R4</td>
<td>390 kΩ Resistor 0402 1% 0.063 W</td>
<td>RC0402FR-07390KL - Yageo</td>
</tr>
<tr>
<td>R5</td>
<td>100 kΩ Resistor 0402 5% 0.1 W</td>
<td>2322-705-70104-L - Yageo</td>
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<tr>
<td>R6</td>
<td>330 kΩ Resistor 0402 1% 0.063 W</td>
<td>RC0402FR-07330KL - Yageo</td>
</tr>
<tr>
<td>U1</td>
<td>Step-Down Regulator MSOP10 3.5 A 2.4 MHz</td>
<td>LT3972IMSE#PBF - Linear Technology</td>
</tr>
</tbody>
</table>

**Table 21: Components for high reliability VCC and 3.3Vaux supply application circuit using a step-down regulator**
Figure 34 and the components listed in Table 22 show an example of a low cost power supply circuit, where the VCC module supply is provided by a step-down switching regulator capable of delivering to VCC pins the specified maximum peak / pulse current, transforming a 12 V supply input.

![Circuit Diagram](image)

**Figure 34: Example of low cost VCC and 3.3Vaux supply application circuit using step-down regulator**

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>22 µF Capacitor Ceramic X5R 1210 10% 25 V</td>
<td>GRM32ER61E226KE15 – Murata</td>
</tr>
<tr>
<td>C2</td>
<td>100 µF Capacitor Tantalum B_SIZE 20% 6.3V 15mΩ</td>
<td>T5208B107M006ATE015 – Kemet</td>
</tr>
<tr>
<td>C3</td>
<td>5.6 nF Capacitor Ceramic X7R 0402 10% 50 V</td>
<td>GRM155R71H562KA88 – Murata</td>
</tr>
<tr>
<td>C4</td>
<td>6.8 nF Capacitor Ceramic X7R 0402 10% 50 V</td>
<td>GRM155R71H682KA88 – Murata</td>
</tr>
<tr>
<td>C5</td>
<td>56 pF Capacitor Ceramic COG 0402 5% 50 V</td>
<td>GRM1555C1H560JA01 – Murata</td>
</tr>
<tr>
<td>C6</td>
<td>220 nF Capacitor Ceramic X7R 0603 10% 25 V</td>
<td>GRM188R71E224KA88 – Murata</td>
</tr>
<tr>
<td>D1</td>
<td>Schottky Diode 25V 2 A</td>
<td>STPS2L25 – STMicroelectronics</td>
</tr>
<tr>
<td>L1</td>
<td>5.2 µH Inductor 30% 5.28A 22 mΩ</td>
<td>MSS1038-522NL – Coilcraft</td>
</tr>
<tr>
<td>R1</td>
<td>4.7 kΩ Resistor 0402 1% 0.063 W</td>
<td>RC0402FR-074K7L – Yageo</td>
</tr>
<tr>
<td>R2</td>
<td>910 Ω Resistor 0402 1% 0.063 W</td>
<td>RC0402FR-07910RL – Yageo</td>
</tr>
<tr>
<td>R3</td>
<td>82 Ω Resistor 0402 5% 0.063 W</td>
<td>RC0402JR-0782RL – Yageo</td>
</tr>
<tr>
<td>R4</td>
<td>8.2 kΩ Resistor 0402 5% 0.063 W</td>
<td>RC0402JR-078K2L – Yageo</td>
</tr>
<tr>
<td>R5</td>
<td>39 kΩ Resistor 0402 5% 0.063 W</td>
<td>RC0402JR-0739KL – Yageo</td>
</tr>
<tr>
<td>R6</td>
<td>1.5 kΩ Resistor 0402 1% 0.063 W</td>
<td>RC0402FR-071K5L – Yageo</td>
</tr>
<tr>
<td>R7</td>
<td>330 Ω Resistor 0402 1% 0.063 W</td>
<td>RC0402FR-07330RL – Yageo</td>
</tr>
<tr>
<td>U1</td>
<td>Step-Down Regulator 8-VFQFPN 3 A 1 MHz</td>
<td>LS987TR – ST Microelectronics</td>
</tr>
</tbody>
</table>

**Table 22: Components for low cost VCC and 3.3Vaux supply application circuit using a step-down regulator**
2.2.1.3 Guidelines for VCC or 3.3Vaux supply circuit design using a Low Drop-Out linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail and the VCC or the 3.3Vaux value is low. The linear regulators provide high efficiency when transforming a 5 VDC supply to a voltage value within the module VCC or 3.3Vaux normal operating range.

The characteristics of the Low Drop-Out (LDO) linear regulator connected to VCC or 3.3Vaux pins should meet the following prerequisites to comply with the module VCC or 3.3Vaux requirements summarized in Table 7:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a voltage value to the VCC or 3.3Vaux pins within the specified operating range and must be capable of delivering to VCC or 3.3Vaux pins the maximum peak / pulse current consumption during Tx burst at maximum Tx power specified in TOBY-L2 series Data Sheet [1] or in MPCI-L2 series Data Sheet [2].

- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (e.g. check the voltage drop from the max input voltage to the minimum output voltage to evaluate the power dissipation of the regulator).

Figure 35 and the components listed in Table 23 show an example of a power supply circuit, where the VCC or 3.3Vaux module supply is provided by an LDO linear regulator capable of delivering the required current, with proper power handling capability.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module VCC or 3.3Vaux normal operating range (e.g. ~4.1 V for the VCC and ~3.44 V for the 3.3Vaux as in the circuits described in Figure 35 and Table 23). This reduces the power on the linear regulator and improves the thermal design of the circuit.

![Figure 35: Suggested schematic design for the VCC and 3.3Vaux supply application circuit using an LDO linear regulator](image)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2</td>
<td>10 µF Capacitor Ceramic X5R 0603 20% 6.3 V</td>
<td>GRM188R60J106ME47 - Murata</td>
</tr>
<tr>
<td>C3</td>
<td>330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ</td>
<td>T520D337M006ATE045 - KEMET</td>
</tr>
<tr>
<td>R1</td>
<td>47 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-0747KL - Yageo Phycomp</td>
</tr>
<tr>
<td>R2</td>
<td>9.1 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-079K1L - Yageo Phycomp</td>
</tr>
<tr>
<td>R3</td>
<td>3.9 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-073K9L - Yageo Phycomp</td>
</tr>
<tr>
<td>R4</td>
<td>3.3 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-073K3L - Yageo Phycomp</td>
</tr>
<tr>
<td>R5</td>
<td>1.8 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-071K8L - Yageo Phycomp</td>
</tr>
<tr>
<td>U1</td>
<td>LDO Linear Regulator ADJ 3.0 A</td>
<td>LT1764AEQ#PBF - Linear Technology</td>
</tr>
</tbody>
</table>

Table 23: Suggested components for VCC and 3.3Vaux supply application circuit using an LDO linear regulator
Figure 36 and the components listed in Table 24 show an example of a low cost power supply circuit, where the VCC module supply is provided by an LDO linear regulator capable of delivering the specified highest peak / pulse current, with proper power handling capability. The regulator described in this example supports a limited input voltage range and it includes internal circuitry for current and thermal protection.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module VCC normal operating range (e.g. ~4.1 V as in the circuit described in Figure 36 and Table 24). This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2</td>
<td>10 µF Capacitor Ceramic X5R 0603 20% 6.3 V</td>
<td>GRM188R60J106ME47 - Murata</td>
</tr>
<tr>
<td>C3</td>
<td>330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ</td>
<td>T520D337M006ATE045 - KEMET</td>
</tr>
<tr>
<td>R1</td>
<td>27 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-0727KL - Yageo Phycomp</td>
</tr>
<tr>
<td>R2</td>
<td>4.7 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-074K7L - Yageo Phycomp</td>
</tr>
<tr>
<td>R3</td>
<td>12 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-0712KL - Yageo Phycomp</td>
</tr>
<tr>
<td>R4</td>
<td>2.7 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-072K7L - Yageo Phycomp</td>
</tr>
<tr>
<td>U1</td>
<td>LDO Linear Regulator ADJ 3.0 A</td>
<td>LP38501ATI-ADJNOPB - Texas Instrument</td>
</tr>
</tbody>
</table>

2.2.1.4 Guidelines for VCC supply circuit design using a rechargeable Li-Ion or Li-Pol battery

Rechargeable Li-Ion or Li-Pol batteries connected to the VCC pins should meet the following prerequisites to comply with the module VCC requirements summarized in Table 7:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its related output circuit connected to the VCC pins must be capable of delivering a pulse current as the maximum peak current consumption during Tx burst at maximum Tx power specified in TOBY-L2 series Data Sheet [1] and must be capable of extensively delivering a DC current as the maximum average current consumption specified in TOBY-L2 series Data Sheet [1]. The maximum discharge current is not always reported in battery data sheets, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.

- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 7 during transmit bursts.
2.2.1.5 Guidelines for VCC supply circuit design using a primary (disposable) battery

The characteristics of a primary (non-rechargeable) battery connected to VCC pins should meet the following prerequisites to comply with the module VCC requirements summarized in Table 7:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its related output circuit connected to the VCC pins must be capable of delivering a pulse current as the maximum peak current consumption during Tx burst at maximum Tx power specified in TOBY-L2 series Data Sheet [1] and must be capable of extensively delivering a DC current as the maximum average current consumption specified in TOBY-L2 series Data Sheet [1]. The maximum discharge current is not always reported in battery data sheets, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.

- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 7 during transmit bursts.

2.2.1.6 Additional guidelines for VCC or 3.3Vaux supply circuit design

To reduce voltage drops, use a low impedance power source. The series resistance of the power supply lines (connected to the modules’ VCC / 3.3Vaux and GND pins) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize power losses.

Three pins are allocated to VCC supply and five pins to 3.3Vaux supply. Several pins are designated for GND connection. Even if all the VCC / 3.3Vaux pins and all the GND pins are internally connected within the module, it is recommended to properly connect all of them to supply the module to minimize series resistance losses.

To avoid voltage drop undershoot and overshoot at the start and end of a transmit burst during a GSM call (when current consumption on the VCC or 3.3Vaux supply can rise up as specified in TOBY-L2 series Data Sheet [1] or in MPCI-L2 series Data Sheet [2]), place a bypass capacitor with large capacitance (at least 100 µF) and low ESR near the VCC pins, for example:

- A 330 µF capacitance, 45 mΩ ESR (e.g. KEMET T520D337M006ATE045, Tantalum Capacitor)

To reduce voltage ripple and noise, improving RF performance especially if the application device integrates an internal antenna, place the following bypass capacitors near the VCC / 3.3Vaux pins:

- A 68 pF capacitor with Self-Resonant Frequency in the 800/900 MHz range (e.g. Murata GRM1555C1H680J) to filter EMI in the RF low frequencies bands
- A 15 pF capacitor with Self-Resonant Frequency in 1800/1900 MHz range (e.g. Murata GRM1555C1E150J) to filter EMI in the RF high frequencies bands
- An 8.2 pF capacitor with Self-Resonant Frequency in 2500/2600 MHz range (e.g. Murata GRM1555C1H8R2D) to filter EMI in the RF very high frequencies band
- A 10 nF capacitor (e.g. Murata GRM155R71C103K) to filter digital logic noise from clocks and data sources
- An 100 nF capacitor (e.g. Murata GRM155R61C104K) to filter digital logic noise from clocks and data sources

A suitable series ferrite bead can be properly placed on the VCC / 3.3Vaux line for additional noise filtering if required by the specific application according to the whole application board design.

The necessity of each part depends on the specific design, but it is recommended to provide all the bypass capacitors described in Figure 37 / Table 25 if the application device integrates an internal antenna.
Figure 37: Suggested schematic for the VCC / 3.3Vaux bypass capacitors to reduce ripple / noise on supply voltage profile

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>68 pF Capacitor Ceramic C0G 0402 5% 50 V</td>
<td>GRM1555C1H680JA01 - Murata</td>
</tr>
<tr>
<td>C2</td>
<td>15 pF Capacitor Ceramic C0G 0402 5% 50 V</td>
<td>GRM1555C1H150JA01 - Murata</td>
</tr>
<tr>
<td>C3</td>
<td>8.2 pF Capacitor Ceramic C0G 0402 5% 50 V</td>
<td>GRM1555C1H820JA01 - Murata</td>
</tr>
<tr>
<td>C4</td>
<td>10 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R71C103KA01 - Murata</td>
</tr>
<tr>
<td>C5</td>
<td>100 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R71C104KA01 - Murata</td>
</tr>
<tr>
<td>C6</td>
<td>330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ</td>
<td>T520D337M006ATE045 - KEMET</td>
</tr>
</tbody>
</table>

Table 25: Suggested components to reduce ripple / noise on VCC / 3.3Vaux

ESD sensitivity rating of the VCC / 3.3Vaux supply pins is 1 kV (HBM according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if accessible battery connector is directly connected to the supply pins. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible point.
### 2.2.1.7 Guidelines for external battery charging circuit

TOBY-L2 modules do not have an on-board charging circuit. Figure 38 provides an example of a battery charger design, suitable for applications that are battery powered with a Li-Ion (or Li-Polymer) cell.

In the application circuit, a rechargeable Li-Ion (or Li-Polymer) battery cell, that features proper pulse and DC discharge current capabilities and proper DC series resistance, is directly connected to the VCC supply input of TOBY-L2 module. Battery charging is completely managed by the STMicroelectronics L6924U Battery Charger IC that, from a USB power source (5.0 V typ.), charges as a linear charger the battery, in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for USB power source (~500 mA)
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the L6924U starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor to ~15 mA or when the charging timer reaches the value configured by an external capacitor to ~9800 s

Using a battery pack with an internal NTC resistor, the L6924U can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Alternatively the L6924U, providing input voltage range up to 12 V, can charge from an AC wall adapter. When a current-limited adapter is used, it can operate in quasi-pulse mode, reducing power dissipation.

![Figure 38: Li-Ion (or Li-Polymer) battery charging application circuit](image)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1</td>
<td>Li-Ion (or Li-Polymer) battery pack with 470 Ω NTC</td>
<td>Various manufacturer</td>
</tr>
<tr>
<td>C1, C4</td>
<td>1 µF Capacitor Ceramic X7R 0603 10% 16 V</td>
<td>GRM188R71C105KA12 - Murata</td>
</tr>
<tr>
<td>C2, C6</td>
<td>10 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R71C103KA01 - Murata</td>
</tr>
<tr>
<td>C3</td>
<td>1 nF Capacitor Ceramic X7R 0402 10% 50 V</td>
<td>GRM155R71H102KA01 - Murata</td>
</tr>
<tr>
<td>C5</td>
<td>330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ</td>
<td>TS20D337M006ATE045 - KEMET</td>
</tr>
<tr>
<td>C7</td>
<td>100 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R61A104KA01 - Murata</td>
</tr>
<tr>
<td>C8</td>
<td>68 pF Capacitor Ceramic C0G 0402 5% 50 V</td>
<td>GRM1555C1H680JA01 - Murata</td>
</tr>
<tr>
<td>C9</td>
<td>15 pF Capacitor Ceramic C0G 0402 5% 50 V</td>
<td>GRM1555C1H150JA01 - Murata</td>
</tr>
<tr>
<td>C10</td>
<td>8.2 pF Capacitor Ceramic C0G 0402 5% 50 V</td>
<td>GRM1555C1H8R2DZ01 - Murata</td>
</tr>
<tr>
<td>D1</td>
<td>Low Capacitance ESD Protection</td>
<td>USB0002RP or USB0002DP - AVX</td>
</tr>
<tr>
<td>R1, R2</td>
<td>24 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-0724KL - Yageo Phycomp</td>
</tr>
<tr>
<td>R3</td>
<td>3.3 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-073K3L - Yageo Phycomp</td>
</tr>
<tr>
<td>R4</td>
<td>1.0 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-071K0L - Yageo Phycomp</td>
</tr>
<tr>
<td>U1</td>
<td>Single Cell Li-Ion (or Li-Polymer) Battery Charger IC</td>
<td>L6924U - STMicroelectronics</td>
</tr>
</tbody>
</table>

**Table 26: Suggested components for Li-Ion (or Li-Polymer) battery charging application circuit**
2.2.1.8 Guidelines for external battery charging and power path management circuit

Application devices where both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source should implement a suitable charger / regulator with integrated power path management function to supply the module and the whole device while simultaneously and independently charging the battery.

Figure 39 reports a simplified block diagram circuit showing the working principle of a charger / regulator with integrated power path management function. This component allows the system to be powered by a permanent primary supply source (e.g. ~12 V) using the integrated regulator which simultaneously and independently recharges the battery (e.g. 3.7 V Li-Pol) that represents the back-up supply source of the system: the power path management feature permits the battery to supplement the system current requirements when the primary supply source is not available or cannot deliver the peak system currents.

A power management IC should meet the following prerequisites to comply with the module VCC requirements summarized in Table 7:
- High efficiency internal step down converter, compliant with the performances specified in section 2.2.1.2
- Low internal resistance in the active path Vout – Vbat, typically lower than 50 mΩ
- High efficiency switch mode charger with separate power path control

![Figure 39: Charger / regulator with integrated power path management circuit block diagram](image)

Figure 40 and the components listed in Table 27 provide an application circuit example where the MPS MP2617 switching charger / regulator with integrated power path management function provides the supply to the cellular module while concurrently and autonomously charging a suitable Li-Ion (or Li-Polymer) battery with proper pulse and DC discharge current capabilities and proper DC series resistance according to the rechargeable battery recommendations described in section 2.2.1.4.

The MP2617 IC constantly monitors the battery voltage and selects whether to use the external main primary supply / charging source or the battery as supply source for the module, and starts a charging phase accordingly.

The MP2617 IC normally provides a supply voltage to the module regulated from the external main primary source allowing immediate system operation even under missing or deeply discharged battery: the integrated switching step-down regulator is capable to provide up to 3 A output current with low output ripple and fixed 1.6 MHz switching frequency in PWM mode operation. The module load is satisfied in priority, then the integrated switching charger will take the remaining current to charge the battery.

Additionally, the power path control allows an internal connection from battery to the module with a low series internal ON resistance (40 mΩ typical), in order to supplement additional power to the module when the current demand increases over the external main primary source or when this external source is removed.
Battery charging is managed in three phases:

- **Pre-charge constant current**: (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current.
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for the application.
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the current is progressively reduced until the charge termination is done. The charging process ends when the charging current reaches the 10% of the fast-charge current or when the charging timer reaches the value configured by an external capacitor.

Using a battery pack with an internal NTC resistor, the MP2617 can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Several parameters as the charging current, the charging timings, the input current limit, the input voltage limit, the system output voltage can be easily set according to the specific application requirements, as the actual electrical characteristics of the battery and the external supply / charging source: proper resistors or capacitors have to be accordingly connected to the related pins of the IC.

![Figure 40: Li-Ion (or Li-Polymer) battery charging and power path management application circuit](image)

**Table 27: Suggested components for Li-Ion (or Li-Polymer) battery charging and power path management application circuit**

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1</td>
<td>Li-Ion (or Li-Polymer) battery pack with 10 kΩ NTC</td>
<td>Various manufacturer</td>
</tr>
<tr>
<td>C1, C5, C6</td>
<td>22 µF Capacitor Ceramic X5R 1210 10% 25 V</td>
<td>GRM32ER61E226KE15 - Murata</td>
</tr>
<tr>
<td>C2, C4, C11</td>
<td>100 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R61A104KA01 - Murata</td>
</tr>
<tr>
<td>C3</td>
<td>1 µF Capacitor Ceramic X7R 0603 10% 25 V</td>
<td>GRM188R71E105KA12 - Murata</td>
</tr>
<tr>
<td>C7, C13</td>
<td>68 pF Capacitor Ceramic COG 0402 5% 50 V</td>
<td>GRM1555C1H680JA01 - Murata</td>
</tr>
<tr>
<td>C8, C14</td>
<td>15 pF Capacitor Ceramic COG 0402 5% 25 V</td>
<td>GRM1555C1E150JA01 - Murata</td>
</tr>
<tr>
<td>C9, C15</td>
<td>8.2 pF Capacitor Ceramic COG 0402 5% 50 V</td>
<td>GRM1555C1H820DZ01 - Murata</td>
</tr>
<tr>
<td>C10</td>
<td>330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ</td>
<td>T520D337M006ATE045 - KEMET</td>
</tr>
<tr>
<td>C12</td>
<td>10 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R71C103KA01 - Murata</td>
</tr>
<tr>
<td>D1, D2</td>
<td>Low Capacitance ESD Protection</td>
<td>CG0402MLE-18G - Bourns</td>
</tr>
<tr>
<td>R1, R3, R5</td>
<td>10 kΩ Resistor 0402 5% 1/16 W</td>
<td>RC0402JR-0710KL - Yageo Phycomp</td>
</tr>
<tr>
<td>R2</td>
<td>1.0 kΩ Resistor 0420 5% 0.1 W</td>
<td>RC0402JR-0710KL - Yageo Phycomp</td>
</tr>
<tr>
<td>R4</td>
<td>22 kΩ Resistor 0420 5% 1/16 W</td>
<td>RC0402JR-0722KL - Yageo Phycomp</td>
</tr>
<tr>
<td>L1</td>
<td>1.2 µH Inductor 6 A 21 mΩ 20%</td>
<td>7447745012 - Wurth</td>
</tr>
<tr>
<td>U1</td>
<td>Li-IonLi-Polymer Battery DC/DC Charger / Regulator with integrated Power Path Management function</td>
<td>MP2617 - Monolithic Power Systems (MPS)</td>
</tr>
</tbody>
</table>
2.2.1.9 Guidelines for VCC or 3.3Vaux supply layout design

Good connection of the module VCC or 3.3Vaux pins with DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available VCC / 3.3Vaux pins must be connected to the DC source
- VCC / 3.3Vaux connection must be as wide as possible and as short as possible
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided
- VCC / 3.3Vaux connection must be routed through a PCB area separated from RF lines / parts, sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between the VCC / 3.3Vaux track and other signal routing
- Coupling between VCC / 3.3Vaux and digital lines, especially USB, must be avoided.
- The tank bypass capacitor with low ESR for current spikes smoothing described in section 2.2.1.6 should be placed close to the VCC / 3.3Vaux pins. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize VCC / 3.3Vaux track length. Otherwise consider using separate capacitors for DC-DC converter and module tank capacitor
- The bypass capacitors in the pF range described in Figure 37 and Table 25 should be placed as close as possible to the VCC / 3.3Vaux pins. This is highly recommended if the application device integrates an internal antenna
- Since VCC / 3.3Vaux input provide the supply to RF Power Amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the TOBY-L2 and MPCI-L2 series modules in the worst case
- If VCC / 3.3Vaux is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the module, preferably closer to the DC source (otherwise protection functionality may be compromised)

2.2.1.10 Guidelines for grounding layout design

Good connection of the module GND pins with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each GND pin with application board solid GND layer. It is strongly recommended that each GND pad surrounding VCC pins have one or more dedicated via down to the application board solid ground layer
- The VCC supply current flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source
- It is recommended to implement one layer of the application board as ground plane as wide as possible
- If the application board is a multilayer PCB, then all the board layers should be filled with GND plane as much as possible and each GND area should be connected together with complete via stack down to the main ground layer of the board. Use as many vias as possible to connect the ground planes
- Provide a dense line of vias at the edges of each ground area, in particular along RF and high speed lines
- If the whole application device is composed by more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the different PCBs
- Good grounding of GND pads also ensures thermal heat sink. This is critical during connection, when the real network commands the module to transmit at maximum power: proper grounding helps prevent module overheating.
### 2.2.2 RTC supply output (V_BCKP)

The RTC supply V_BCKP pin is not available on MPCI-L2 series modules.

#### 2.2.2.1 Guidelines for V_BCKP circuit design

TOBY-L2 series modules provide the V_BCKP RTC supply input/output, which can be mainly used to:

- Provide RTC back-up when VCC supply is removed

If RTC timing is required to run for a time interval of $T$ [s] when VCC supply is removed, place a capacitor with a nominal capacitance of $C$ [$\mu$F] at the V_BCKP pin. Choose the capacitor using the following formula:

$$C = \frac{(Current\_Consumption\ [\mu\text{A}] \times T\ [\text{s}])}{Voltage\_Drop\ [V]} = 1.25 \times T\ [\text{s}]$$

For example, a 100 µF capacitor can be placed at V_BCKP to provide RTC backup holding the V_BCKP voltage within its valid range for around 80 s at 25 °C, after the VCC supply is removed. If a longer buffering time is required, a 70 mF super-capacitor can be placed at V_BCKP, with a 4.7 kΩ series resistor to hold the V_BCKP voltage within its valid range for approximately 15 hours at 25 °C, after the VCC supply is removed. The purpose of the series resistor is to limit the capacitor charging current due to the large capacitor specifications, and also to let a fast rise time of the voltage value at the V_BCKP pin after VCC supply has been provided. These capacitors allow the time reference to run during battery disconnection.

![Figure 41: Real time clock supply (V_BCKP) application circuits](image)

(a) TOBY-L2 series  
(b) TOBY-L2 series  
(c) TOBY-L2 series

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>100 µF Tantalum Capacitor</td>
<td>GRM43SR60J107M - Murata</td>
</tr>
<tr>
<td>R2</td>
<td>4.7 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-074K7L - Yageo Phycomp</td>
</tr>
<tr>
<td>C2</td>
<td>70 mF Capacitor</td>
<td>XH414H-IV01E - Seiko Instruments</td>
</tr>
</tbody>
</table>

Table 28: Example of components for V_BCKP buffering

If very long buffering time is required to allow the RTC time reference to run during a disconnection of the VCC supply, then an external battery can be connected to V_BCKP pin. The battery should be able to provide a proper nominal voltage and must never exceed the maximum operating voltage for V_BCKP (specified in the input characteristics of Supply/Power pins table in TOBY-L2 series Data Sheet [1]). The connection of the battery to V_BCKP should be done with a suitable series resistor for a rechargeable battery, or with an appropriate series diode for a non-rechargeable battery. The purpose of the series resistor is to limit the battery charging current due to the battery specifications, and also to allow a fast rise time of the voltage value at the V_BCKP pin after the VCC supply has been provided. The purpose of the series diode is to avoid a current flow from the module V_BCKP pin to the non-rechargeable battery.
If the RTC timing is not required when the VCC supply is removed, it is not needed to connect the V_BCKP pin to an external capacitor or battery. In this case the date and time are not updated when VCC is disconnected. If VCC is always supplied, then the internal regulator is supplied from the main supply and there is no need for an external component on V_BCKP.

V_BCKP supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

Do not apply loads which might exceed the limit for maximum available current from V_BCKP supply (see TOBY-L2 series Data Sheet [1]) as this can cause malfunctions in internal circuitry.

ESD sensitivity rating of the V_BCKP supply pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the line is externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible point.

2.2.2.2 Guidelines for V_BCKP layout design

V_BCKP supply requires careful layout: avoid injecting noise on this voltage domain as it may affect the stability of the internal circuitry.
2.2.3  Generic digital interfaces supply output (V_INT)

The generic digital interfaces supply V_INT pin is not available on MPCI-L2 series modules.

2.2.3.1  Guidelines for V_INT circuit design

TOBY-L2 series provide the V_INT generic digital interfaces 1.8 V supply output, which can be mainly used to:

- Indicate when the module is switched on (as described in sections 1.6.1, 1.6.2)
- Pull-up SIM detection signal (see section 2.5 for more details)
- Supply voltage translators to connect 1.8 V module generic digital interfaces to 3.0 V devices (e.g. see 2.6.2)
- Pull-up DDC (I²C) interface signals (see section 2.6.3 for more details)
- Enable external voltage regulators providing supply for external devices, as linear LDO regulators providing the 3.3 V / 1.8 V supply rails for a u-blox ELLA-W1 series module (see section 2.6.4 for more details)
- Supply an external device, as an external 1.8 V audio codec (see section 2.7.1 for more details)

V_INT supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

Do not apply loads which might exceed the limit for maximum available current from V_INT supply (see the TOBY-L2 series Data Sheet [1]) as this can cause malfunctions in internal circuitry.

Since the V_INT supply is generated by an internal switching step-down regulator, the V_INT voltage ripple can range as specified in the TOBY-L2 series Data Sheet [1]: it is not recommended to supply sensitive analog circuitry without adequate filtering for digital noise.

V_INT can only be used as an output: do not connect any external supply source on V_INT.

ESD sensitivity rating of the V_INT supply pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the line is externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible point.

It is recommended to provide direct access to the V_INT pin on the application board by means of an accessible test point directly connected to the V_INT pin.

2.2.3.2  Guidelines for V_INT layout design

V_INT supply output is generated by an integrated switching step-down converter. Because of this, it can be a source of noise: avoid coupling with sensitive signals.
2.3 System functions interfaces

2.3.1 Module power-on (PWR_ON)

The PWR_ON input pin is not available on MPCI-L2 series modules.

2.3.1.1 Guidelines for PWR_ON circuit design

TOBY-L2 series PWR_ON input is equipped with an internal active pull-up resistor to the VCC module supply as described in Figure 42: an external pull-up resistor is not required and should not be provided.

If connecting the PWR_ON input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection should be provided close to the accessible point, as described in Figure 42 and Table 29.

ESD sensitivity rating of the PWR_ON pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to PWR_ON pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA0SP4S14THSG varistor) close to the accessible point.

An open drain or open collector output is suitable to drive the PWR_ON input from an application processor as PWR_ON input is equipped with an internal active pull-up resistor to the VCC supply, as described in Figure 42. A compatible push-pull output of an application processor can also be used. In any case, take care to set the proper level in all the possible scenarios to avoid an inappropriate module switch-on.

![Figure 42: PWR_ON application circuits using a push button and an open drain output of an application processor](image)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD</td>
<td>CT0402S14AHSG - EPCOS</td>
<td>Varistor array for ESD protection</td>
</tr>
</tbody>
</table>

Table 29: Example ESD protection component for the PWR_ON application circuit

It is recommended to provide direct access to the PWR_ON pin on the application board by means of an accessible test point directly connected to the PWR_ON pin.

2.3.1.2 Guidelines for PWR_ON layout design

The power-on circuit (PWR_ON) requires careful layout since it is the sensitive input available to switch on the TOBY-L2 modules. It is required to ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.
2.3.2 Module reset (RESET_N or PERST#)

2.3.2.1 Guidelines for RESET_N and PERST# circuit design

The TOBY-L2 series RESET_N is equipped with an internal pull-up to the VCC supply and the MPCI-L2 series PERST# is equipped with an internal pull-up to the 3.3 V rail, as described in Figure 43. An external pull-up resistor is not required and should not be provided.

If connecting the RESET_N or PERST# input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device (e.g. the EPCOS CA05P4S14THSG varistor) should be provided close to accessible point on the line connected to this pin, as described in Figure 43 and Table 30.

ESD sensitivity rating of the RESET_N and PERST# pins is 1 kV (HBM according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the RESET_N or PERST# pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible point.

An open drain output is suitable to drive the RESET_N and PERST# inputs from an application processor as they are equipped with an internal pull-up to VCC supply and to the 3.3 V rail respectively, as described in Figure 43.

A compatible push-pull output of an application processor can also be used. In any case, take care to set the proper level in all the possible scenarios to avoid an inappropriate module reset, switch-on or switch-off.

If the external reset function is not required by the customer application, the RESET_N input pin can be left unconnected to external components, but it is recommended providing direct access on the application board by means of an accessible test point directly connected to the RESET_N pin.

![Figure 43: RESET_N and PERST# application circuits using a push button and an open drain output of an application processor](image-url)
2.3.2.2 Guidelines for RESET_N and PERST# layout design
The RESET_N and PERST# circuits require careful layout due to the pin function: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious reset request. It is recommended to keep the connection line to RESET_N and PERST# pins as short as possible.

2.3.3 Module configuration selection by host processor

The HOST_SELECT0 and HOST_SELECT1 pins are not available on MPCI-L2 series modules.

2.3.3.1 Guidelines for HOST_SELECTx circuit design

The functionality of HOST_SELECT0 and HOST_SELECT1 pins is not supported by all the TOBY-L2 series modules product versions: the two input pins should not be driven by the host application processor or any other external device.

TOBY-L2 series modules include two input pins (HOST_SELECT0 and HOST_SELECT1) for the selection of the module configuration by the host application processor.

- Do not apply voltage to HOST_SELECT0 and HOST_SELECT1 pins before the switch-on of their supply source (V_INT), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. TI SN74CB3Q16244, T5SA3159, or T5SA63157) between the two circuit connections and set to high impedance before V_INT switch-on.

- ESD sensitivity rating of the HOST_SELECT0 and HOST_SELECT1 pins is 1 kV (HBM as per JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

- If the HOST_SELECT0 and HOST_SELECT1 pins are not used, they can be left unconnected on the application board.

2.3.3.2 Guidelines for HOST_SELECTx layout design

The input pins for the selection of the module configuration by the host application processor (HOST_SELECT0 and HOST_SELECT1) are generally not critical for layout.
2.4 Antenna interface

TOBY-L2 and MPCI-L2 series modules provide two RF interfaces for connecting the external antennas:
- The **ANT1** pin represents the primary RF input/output for LTE/3G/2G RF signals transmission and reception.
- The **ANT2** pin represents the secondary RF input for LTE MIMO 2 x 2 or 3G Rx diversity RF signals reception.

Both the **ANT1** and the **ANT2** pins have a nominal characteristic impedance of 50 Ω and must be connected to the related antenna through a 50 Ω transmission line to allow proper transmission / reception of RF signals.

Two antennas (one connected to **ANT1** pin and one connected to **ANT2** pin) must be used to support the Down-Link MIMO 2 x 2 radio technology. This is a required feature for LTE category 4 User Equipments (up to 150 Mb/s Down-Link data rate) according to 3GPP specifications.

2.4.1 Antenna RF interfaces (ANT1 / ANT2)

2.4.1.1 General guidelines for antenna selection and design

The antenna is the most critical component to be evaluated. Designers must take care of the antennas from all perspective at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating TOBY-L2 and MPCI-L2 series modules with all the applicable required certification schemes depends on antennas radiating performance.

LTE/3G/2G antennas are typically available in the types of linear monopole or PCB antennas such as patches or ceramic SMT elements.
- External antennas (e.g. linear monopole):
  - External antennas basically do not imply physical restriction to the design of the PCB where the TOBY-L2 and MPCI-L2 series module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected to have minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces both transmit and receive radiation performance.
  - A high quality 50 Ω RF connector provides proper PCB-to-RF-cable transition. It is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
- Integrated antennas (e.g. patch-like antennas):
  - Internal integrated antennas imply physical restriction to the design of the PCB:
    Integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna: its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that has to be radiated, given that the orientation of the ground plane relative to the antenna element must be considered.
    The isolation between the primary and the secondary antennas has to be as high as possible and the correlation between the 3D radiation patterns of the two antennas has to be as low as possible. In general, a separation of at least a quarter wavelength between the two antennas is required to achieve a good isolation and low pattern correlation.
    As numerical example, the physical restriction to the PCB design can be considered as following:
    - Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm
Radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.

It is recommended to select a pair of custom antennas designed by an antenna manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide). The antenna design process should begin at the start of the whole product design process.

It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.

Further to the custom PCB and product restrictions, antennas may require tuning to obtain the required performance for compliance with all the applicable certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for antenna matching relative to the custom application.

In both of cases, selecting external or internal antennas, these recommendations should be observed:

- Select antennas providing optimal return loss (or V.S.W.R.) figure over all the operating frequencies.
- Select antennas providing optimal efficiency figure over all the operating frequencies.
- Select antennas providing similar efficiency for both the primary (ANT1) and the secondary (ANT2) antenna.
- Select antennas providing appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity do not exceed the regulatory limits specified in some countries (e.g. by FCC in the United States, as reported in the section 4.2.2).
- Select antennas capable to provide low Envelope Correlation Coefficient between the primary (ANT1) and the secondary (ANT2) antenna: the 3D antenna radiation patterns should have lobes in different directions.

2.4.1.2 Guidelines for antenna RF interface design

Guidelines for TOBY-L2 series ANT1 / ANT2 pins RF connection design

Proper transition between ANT1 / ANT2 pads and the application board PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the ANT1 / ANT2 pads:

- On a multilayer board, the whole layer stack below the RF connection should be free of digital lines.
- Increase GND keep-out (i.e. clearance, a void area) around the ANT1 / ANT2 pads, on the top layer of the application PCB, to at least 250 µm up to adjacent pads metal definition and up to 400 µm on the area below the module, to reduce parasitic capacitance to ground, as described in the left picture in Figure 44.
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the ANT1 / ANT2 pads if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as described in the right picture in Figure 44.

![Figure 44: GND keep-out area on top layer around ANT1 / ANT2 pads and on very close buried layer below ANT1 / ANT2 pads](image_url)
**Guidelines for MPCI-L2 series ANT1 / ANT2 receptacles RF connection design**

The Hirose U.FL-R-SMT RF receptacles implemented on the MPCI-L2 series modules for ANT1 / ANT2 ports require a suitable mated RF plug from the same connector series. Due to its wide usage in the industry, several manufacturers offer compatible equivalents.

Table 31 lists some RF connector plugs that fit MPCI-L2 series modules RF connector receptacles, based on the declaration of the respective manufacturers. Only the Hirose has been qualified for the MPCI-L2 series modules; contact other producers to verify compatibility.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Series</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hirose</td>
<td>U.FL® Ultra Small Surface Mount Coaxial Connector</td>
<td>Recommended</td>
</tr>
<tr>
<td>I-PEX</td>
<td>MHF® Micro Coaxial Connector</td>
<td></td>
</tr>
<tr>
<td>Tyco</td>
<td>UMCC® Ultra-Miniature Coax Connector</td>
<td></td>
</tr>
<tr>
<td>Amphenol RF</td>
<td>AMC® Amphenol Micro Coaxian</td>
<td></td>
</tr>
<tr>
<td>Lighthorse Technologies, Inc</td>
<td>IPX ultra micro-miniature RF connector</td>
<td></td>
</tr>
</tbody>
</table>

Table 31: MPCI-L2 series U.FL compatible plug connector

Typically the RF plug is available as a cable assembly: several kinds are available and the user should select the cable assembly best suited to the application. The key characteristics are:

- RF plug type: select U.FL or equivalent
- Nominal impedance: 50 Ω
- Cable thickness: typically from 0.8 mm to 1.37 mm. Select thicker cables to minimize insertion loss
- Cable length: standard length is typically 100 mm or 200 mm, custom lengths may be available on request. Select shorter cables to minimize insertion loss
- RF connector on the other side of the cable: for example another U.FL (for board-to-board connection) or SMA (for panel mounting)

For applications requiring an internal integrated SMT antenna, it is suggested to use a U-FL-to-U.FL cable to provide RF path from the MPCI-L2 series module to PCB strip line or micro strip connected to antenna pads as shown in Figure 45. Take care that the PCB-to-RF-cable transition, strip line and antenna pads must be designed so that the characteristic impedance is as close as possible to 50 Ω: see the following subsections for specific guidelines regarding RF transmission line design and RF termination design.

If an external antenna is required, consider that the connector is typically rated for a limited number of insertion cycles. In addition, the RF coaxial cable may be relatively fragile compared to other types of cables. To increase application ruggedness, connect U.FL to a more robust connector (e.g. SMA or MMCX) fixed on panel or on flange as shown in Figure 45.

![Figure 45: Example of RF connections, U.FL-to-U.FL cable for internal antenna and U.FL-to-SMA for external antenna](image-url)
Guidelines for RF transmission line design

Any RF transmission line, such as the ones from the ANT1 and ANT2 pads up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω.

RF transmission lines can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

Figure 46 and Figure 47 provide two examples of proper 50 Ω coplanar waveguide designs. The first example of RF transmission line can be implemented in case of 4-layer PCB stack-up herein described, and the second example of RF transmission line can be implemented in case of 2-layer PCB stack-up herein described.

If the two examples do not match the application PCB stack-up the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like AppCAD from Agilent (www.agilent.com) or TXLine from Applied Wave Research (www.mwoffice.com), taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the width of the transmission line must be chosen depending on:

- the thickness of the transmission line itself (e.g. 35 μm in the example of Figure 46 and Figure 47)
- the thickness of the dielectric material between the top layer (where the transmission line is routed) and the inner closer layer implementing the ground plane (e.g. 270 μm in Figure 46, 1510 μm in Figure 47)
- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 46 and Figure 47)
• the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 46, 400 µm in Figure 47)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the “Coplanar Waveguide” model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for transmission lines design:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB,
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission lines, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground,
- The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND,
- Add GND stitching vias around transmission lines, as described in Figure 48,
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough vias on the adjacent metal layer, as described in Figure 48,
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as USB),
- Avoid stubs on the transmission lines,
- Avoid signal routing in parallel to transmission lines or crossing the transmission lines on buried metal layer,
- Do not route microstrip lines below discrete component or other mechanics placed on top layer

An example of proper RF circuit design is reported in Figure 48. In this case, the ANT1 and ANT2 pins are directly connected to SMA connectors by means of proper 50 Ω transmission lines, designed with proper layout.

Figure 48: Suggested circuit and layout for antenna RF circuits on application board
Guidelines for RF termination design

RF terminations must provide a characteristic impedance of 50 Ω as well as the RF transmission lines up to the RF terminations themselves, to match the characteristic impedance of the ANT1 / ANT2 ports of the modules.

However, real antennas do not have perfect 50 Ω load on all the supported frequency bands. Therefore, to reduce as much as possible performance degradation due to antennas mismatch, RF terminations must provide optimal return loss (or V.S.W.R.) figure over all the operating frequencies, as summarized in Table 8 and Table 9.

If external antennas are used, the antenna connectors represent the RF termination on the PCB:
- Use suitable 50 Ω connectors providing proper PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer’s recommended layout, for example:
  - SMA Pin-Through-Hole connectors require GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to annular pads of the four GND posts, as shown in Figure 48
  - U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads.
- Cut out the GND layer under RF connectors and close to buried vias, to remove stray capacitance and thus keep the RF line 50 Ω, e.g. the active pad of UFL connectors needs to have a GND keep-out (i.e. clearance, a void area) at least on first inner layer to reduce parasitic capacitance to ground.

If integrated antennas are used, the RF terminations are represented by the integrated antennas themselves. The following guidelines should be followed:
- Use antennas designed by an antenna manufacturer, providing the best possible return loss (or V.S.W.R.).
- Provide a ground plane large enough according to the relative integrated antenna requirements. The ground plane of the application PCB can be reduced down to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated. As numerical example,
  Frequency = 750 MHz \rightarrow \text{Wavelength} = 40 \text{ cm} \rightarrow \text{Minimum GND plane size} = 10 \text{ cm}
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require a tuning to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for the antenna matching relative to the custom application.

Additionally, these recommendations regarding the antenna system placement must be followed:
- Do not place antennas within closed metal case.
- Do not place the antennas in close vicinity to end user since the emitted radiation in human tissue is limited by regulatory requirements.
- Place the antennas far from sensitive analog systems or employ countermeasures to reduce EMC issues.
- Take care of interaction between co-located RF systems since the LTE/3G/2G transmitted power may interact or disturb the performance of companion systems.
- Place the two LTE/3G antennas providing low Envelope Correlation Coefficient (ECC) between primary (ANT1) and secondary (ANT2) antenna: the antenna 3D radiation patterns should have lobes in different directions. The ECC between primary and secondary antenna needs to be enough low to comply with the radiated performance requirements specified by related certification schemes, as indicated in Table 10.
- Place the two LTE/3G antennas providing enough high isolation (see Table 10) between primary (ANT1) and secondary (ANT2) antenna. The isolation depends on the distance between antennas (separation of at least a quarter wavelength required for good isolation), antenna type (using antennas with different polarization improves isolation), antenna 3D radiation patterns (uncorrelated patterns improve isolation).
Examples of antennas

Table 32 lists some examples of possible internal on-board surface-mount antennas.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Product Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Taoglas</td>
<td>PA.710.A</td>
<td>Warrior</td>
<td>GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm</td>
</tr>
<tr>
<td>Taoglas</td>
<td>PA.711.A</td>
<td>Warrior II</td>
<td>GSM / WCDMA / LTE SMD Antenna Pairs with the Taoglas PA.710.A Warrior for LTE MIMO applications 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm</td>
</tr>
<tr>
<td>Taoglas</td>
<td>PCS.06.A</td>
<td>Havok</td>
<td>GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2500..2690 MHz 42.0 x 10.0 x 3.0 mm</td>
</tr>
<tr>
<td>Antenova</td>
<td>SR4L002</td>
<td>Lucida</td>
<td>GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 35.0 x 8.5 x 3.2 mm</td>
</tr>
</tbody>
</table>

Table 32: Examples of internal surface-mount antennas

Table 33 lists some examples of possible internal off-board PCB-type antennas with cable and connector.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Product Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Taoglas</td>
<td>FXUB63.07.0150C</td>
<td>Maximus</td>
<td>GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1390..1435 MHz, 1575..42 MHz, 1710..2170 MHz, 2400..2700 MHz, 3400..3600 MHz, 4800..6000 MHz 120.2 x 50.4 mm</td>
</tr>
<tr>
<td>Taoglas</td>
<td>FXUB66.07.0150C</td>
<td>Maximus</td>
<td>GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1390..1435 MHz, 1575..42 MHz, 1710..2170 MHz, 2400..2700 MHz, 3400..3600 MHz, 4800..6000 MHz, 968..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 96.0 x 21.0 mm</td>
</tr>
<tr>
<td>Taoglas</td>
<td>FXUB70.A.07.C.001</td>
<td>Maximus</td>
<td>GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1575..42 MHz, 1710..2170 MHz, 2400..2690 MHz 182.2 x 21.2 mm</td>
</tr>
<tr>
<td>Ethertronics</td>
<td>5001537</td>
<td>Prestta</td>
<td>GSM / WCDMA / LTE SMD Antenna 704..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2500..2690 MHz 80.0 x 18.0 mm</td>
</tr>
<tr>
<td>EAD</td>
<td>FSQS35241-UF-10</td>
<td>SQ7</td>
<td>GSM / WCDMA / LTE SMD Antenna 690..960 MHz, 1710..2170 MHz, 2500..2700 MHz 110.0 x 21.0 mm</td>
</tr>
</tbody>
</table>

Table 33: Examples of internal antennas with cable and connector
Table 34 lists some examples of possible external antennas.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Product Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Taoglas</td>
<td>GSA.8827.A.101111</td>
<td>Phoenix</td>
<td>GSM / WCDMA / LTE adhesive-mount antenna with cable and SMA(M) 698.960 MHz, 1575.42 MHz, 1710.2170 MHz, 2490..2690 MHz 105 x 30 x 7.7 mm</td>
</tr>
<tr>
<td>Taoglas</td>
<td>TG.30.8112</td>
<td></td>
<td>GSM / WCDMA / LTE swivel dipole antenna with SMA(M) 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2700 MHz 148.6 x 49 x 10 mm</td>
</tr>
<tr>
<td>Taoglas</td>
<td>MA241.BI.001</td>
<td>Genesis</td>
<td>GSM / WCDMA / LTE MIMO 2in1 adhesive-mount combination antenna waterproof IP67 rated with cable and SMA(M) 698..960 MHz, 1710..2170 MHz, 2400..2700 MHz 205.8 x 58 x 12.4 mm</td>
</tr>
<tr>
<td>Laird Tech.</td>
<td>TRA6927M3PW-001</td>
<td></td>
<td>GSM / WCDMA / LTE screw-mount antenna with N-type(F) 698.960 MHz, 1710..2170 MHz, 2300..2700 MHz 83.8 x Ø 36.5 mm</td>
</tr>
<tr>
<td>Laird Tech.</td>
<td>CMS69273</td>
<td></td>
<td>GSM / WCDMA / LTE ceiling-mount antenna with cable and N-type(F) 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 86 x Ø 199 mm</td>
</tr>
<tr>
<td>Laird Tech.</td>
<td>OC69271-FNM</td>
<td></td>
<td>GSM / WCDMA / LTE pole-mount antenna with N-type(M) 698.960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm</td>
</tr>
<tr>
<td>Laird Tech.</td>
<td>CMD69273-30NM</td>
<td></td>
<td>GSM / WCDMA / LTE ceiling-mount MIMO antenna with cables &amp; N-type(M) 698..960 MHz, 1710..2700 MHz 43.5 x Ø 218.7 mm</td>
</tr>
<tr>
<td>Pulse Electronics</td>
<td>WA700/2700SMA</td>
<td></td>
<td>GSM / WCDMA / LTE clip-mount MIMO antenna with cables and SMA(M) 698..960 MHz, 1710..2700 MHz 149 x 127 x 5.1 mm</td>
</tr>
</tbody>
</table>

Table 34: Examples of external antennas
2.4.2 Antenna detection interface (ANT_DET)

Antenna detection (ANT_DET) is not available on MPCI-L2 series modules

Antenna detection (ANT_DET) is not supported by TOBY-L2 “00”, “01” and “60” product versions

2.4.2.1 Guidelines for ANT_DET circuit design

Figure 49 and Table 35 describe the recommended schematic / components for the antennas detection circuit that must be provided on the application board and for the diagnostic circuit that must be provided on the antennas’ assembly to achieve primary and secondary antenna detection functionality.

The antenna detection circuit and diagnostic circuit suggested in Figure 49 and Table 35 are explained here:

- When antenna detection is forced by AT+UANTR command, ANT_DET generates a DC current measuring the resistance (R2 // R3) from antenna connectors (J1, J2) provided on the application board to GND.
- DC blocking capacitors are needed at the ANT1 / ANT2 pins (C2, C3) and at the antenna radiating element (C4, C5) to decouple the DC current generated by the ANT_DET pin.
- Choke inductors with a Self Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the ANT_DET pin (L1, L2) and in series at the diagnostic resistor (L3, L4), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Additional components (R1, C1 and D1 in Figure 49) are needed at the ANT_DET pin as ESD protection.
- The ANT1 / ANT2 pins must be connected to the antenna connector by means of a transmission line with nominal characteristics impedance as close as possible to 50 Ω.

![Figure 49: Suggested schematic for antenna detection circuit on application board and diagnostic circuit on antennas assembly](image-url)

Table 35: Suggested components for antenna detection circuit on application board and diagnostic circuit on antennas assembly

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>27 pF Capacitor Ceramic COG 0402 5% 50 V</td>
<td>GRM1555C1H270J - Murata</td>
</tr>
<tr>
<td>C2, C3</td>
<td>33 pF Capacitor Ceramic COG 0402 5% 50 V</td>
<td>GRM1555C1H330J - Murata</td>
</tr>
<tr>
<td>D1</td>
<td>Very Low Capacitance ESD Protection</td>
<td>PESD0402-140 - Tyco Electronics</td>
</tr>
<tr>
<td>L1, L2</td>
<td>68 nH Multilayer Inductor 0402 (SRF ~1 GHz)</td>
<td>LQG15H568N02 - Murata</td>
</tr>
<tr>
<td>R1</td>
<td>10 kΩ Resistor 0402 1% 0.063 W</td>
<td>RK73H1ETTP1002F - KOA Speer</td>
</tr>
<tr>
<td>J1, J2</td>
<td>SMA Connector 50 Ω Through Hole Jack</td>
<td>SMA6251A1-3GT50G-50 - Amphenol</td>
</tr>
<tr>
<td>C4, C5</td>
<td>22 pF Capacitor Ceramic COG 0402 5% 25 V</td>
<td>GRM1555C1H220J - Murata</td>
</tr>
<tr>
<td>L3, L4</td>
<td>68 nH Multilayer Inductor 0402 (SRF ~1 GHz)</td>
<td>LQG15H568N02 - Murata</td>
</tr>
<tr>
<td>R2, R3</td>
<td>15 kΩ2 Resistor for Diagnostic</td>
<td>Various Manufacturers</td>
</tr>
</tbody>
</table>
The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 49, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no means to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:
Consider an antenna with built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is properly connected.
- Values close to the measurement range maximum limit (approximately 50 kΩ) or an open-circuit “over range” report (see u-blox AT Commands Manual [3]) means that that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit (1 kΩ) highlights a short to GND at antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an improper connection, damaged antenna or wrong value of antenna load resistor for diagnostic.
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity and the used measurement method.

If the primary / secondary antenna detection function is not required by the customer application, the ANT_DET pin can be left not connected and the ANT1 / ANT2 pins can be directly connected to the related antenna connector by means of a 50 Ω transmission line as described in Figure 48.

### 2.4.2.2 Guidelines for ANT_DET layout design

The recommended layout for the primary antenna detection circuit to be provided on the application board to achieve the primary antenna detection functionality, implementing the recommended schematic described in Figure 49 and Table 35, is explained here:

- The ANT1 / ANT2 pins have to be connected to the antenna connector by means of a 50 Ω transmission line, implementing the design guidelines described in section 2.4.1 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at ANT1 / ANT2 pins (C2, C3) has to be placed in series to the 50 Ω RF line.
- The ANT_DET pin has to be connected to the 50 Ω transmission line by means of a sense line.
- Choke inductors in series at the ANT_DET pin (L1, L2) have to be placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the ANT_DET pin.
- The additional components (R1, C1 and D1) on the ANT_DET line have to be placed as ESD protection.
2.5 SIM interface

SIM detection interface (GPIO5) is not available on the MPCI-L2 series modules.

SIM detection interface (GPIO5) is not supported by the TOBY-L2 modules “00”, “01” and “60” product versions: the pin should not be driven by any external device.

2.5.1 Guidelines for SIM circuit design

Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC), which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the LTE/3G/2G network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221 as follows:

- Contact C1 = VCC (Supply) → It must be connected to VSIM or UIM_PWR
- Contact C2 = RST (Reset) → It must be connected to SIM_RST or UIM_RESET
- Contact C3 = CLK (Clock) → It must be connected to SIM_CLK or UIM_CLK
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to GND
- Contact C6 = VPP (Programming supply) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to SIM_IO or UIM_DATA
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1, C2, C3, C5, C6, C7) or 8 contacts, also including the auxiliary contacts C4 and C8. Only 6 contacts are required and must be connected to the module SIM interface.

Removable SIM cards are suitable for applications requiring a change of SIM card during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins relative to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided. Select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature (not available on MPCI-L2 series) is required by the custom application, otherwise a connector without integrated mechanical presence switch can be selected.

Solderable UICC / SIM chip contact mapping (M2M UICC Form Factor) is defined by ETSI TS 102 671 as:

- Case Pin 8 = UICC Contact C1 = VCC (Supply) → It must be connected to VSIM or UIM_PWR
- Case Pin 7 = UICC Contact C2 = RST (Reset) → It must be connected to SIM_RST or UIM_RESET
- Case Pin 6 = UICC Contact C3 = CLK (Clock) → It must be connected to SIM_CLK or UIM_CLK
- Case Pin 5 = UICC Contact C4 = AUX1 (Aux.contact) → It must be left not connected
- Case Pin 1 = UICC Contact C5 = GND (Ground) → It must be connected to GND
- Case Pin 2 = UICC Contact C6 = VPP (Progr. supply) → It can be left not connected
- Case Pin 3 = UICC Contact C7 = I/O (Data I/O) → It must be connected to SIM_IO or UIM_DATA
- Case Pin 4 = UICC Contact C8 = AUX2 (Aux. contact) → It must be left not connected

A solderable SIM chip has 8 contacts and can also include the auxiliary contacts C4 and C8 for other uses, but only 6 contacts are required and must be connected to the module SIM card interface as described above.

Solderable SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.
Guidelines for single SIM card connection without detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of TOBY-L2 and MPCI-L2 series modules as described in Figure 50, where the optional SIM detection feature is not implemented. Follow these guidelines to connect the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the VSIM / UIM_PWR pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the SIM_IO / UIM_DATA pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the SIM_CLK / UIM_CLK pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the SIM_RST / UIM_RESET pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) on SIM supply line, close to the relative pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco PESD0402-140) on each externally accessible SIM line, close to each relative pad of the SIM connector. ESD sensitivity rating of the SIM interface pins is 1 kV (HBM). So that, according to EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device.
- Limit capacitance and series resistance on each SIM signal to match the SIM requirements (26.2 ns is the maximum allowed rise time on clock line, 1.0 µs is the maximum allowed rise time on data and reset lines).

![Figure 50: Application circuits for the connection to a single removable SIM card, with SIM detection not implemented](image)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2, C3, C4</td>
<td>47 pF Capacitor Ceramic C0G 0402 5% 50 V</td>
<td>GRM1555C1H470J01 - Murata</td>
</tr>
<tr>
<td>C5</td>
<td>100 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R71C104KA01 - Murata</td>
</tr>
<tr>
<td>D1, D2, D3, D4</td>
<td>Very Low Capacitance ESD Protection</td>
<td>PESD0402-140 - Tyco Electronics</td>
</tr>
<tr>
<td>J1</td>
<td>SIM Card Holder, 6 p, without card presence switch</td>
<td>Various manufacturers, as C707 10M006 136 2 - Amphenol</td>
</tr>
</tbody>
</table>

Table 36: Example of components for the connection to a single removable SIM card, with SIM detection not implemented
Guidelines for single SIM chip connection

A solderable SIM chip (M2M UICC Form Factor) must be connected to the SIM card interface of TOBY-L2 and MPCI-L2 series modules as described in Figure 51.

Follow these guidelines to connect the module to a solderable SIM chip without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the VSIM / UIM_PWR pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the SIM_IO / UIM_DATA pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the SIM_CLK / UIM_CLK pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the SIM_RST / UIM_RESET pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line close to the relative pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM lines.
- Limit capacitance and series resistance on each SIM signal to match the SIM requirements (26.2 ns is the maximum allowed rise time on clock line, 1.0 µs is the maximum allowed rise time on data and reset lines).

Figure 51: Application circuits for the connection to a single solderable SIM chip, with SIM detection not implemented

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2, C3, C4</td>
<td>47 pF Capacitor Ceramic C0G 0402 5% 50 V</td>
<td>GRM1555C1H470JA01 - Murata</td>
</tr>
<tr>
<td>C5</td>
<td>100 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R71C104KA01 - Murata</td>
</tr>
<tr>
<td>U1</td>
<td>SIM chip (M2M UICC Form Factor)</td>
<td>Various Manufacturers</td>
</tr>
</tbody>
</table>

Table 37: Example of components for the connection to a single solderable SIM chip, with SIM detection not implemented
Guidelines for single SIM card connection with detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of TOBY-L2 modules as described in Figure 52, where the optional SIM card detection feature is implemented.

Follow these guidelines to connect the module to a SIM connector implementing SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the VSIM pin of the module.
- Connect the UICC / SIM contact C7 (IO) to the SIM_IO pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the SIM_CLK pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the SIM_RST pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Connect one pin of the normally-open mechanical switch integrated in the SIM connector (e.g. the SW2 pin as described in Figure 52) to the GPOI5 input pin of the module.
- Connect the other pin of the normally-open mechanical switch integrated in the SIM connector (e.g. the SW1 pin as described in Figure 52) to the V_INT 1.8 V supply output of the module by means of a strong (e.g. 1 kΩ) pull-up resistor, as the R1 resistor in Figure 52.
- Provide a weak (e.g. 470 kΩ) pull-down resistor at the SIM detection line, as the R2 resistor in Figure 52.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line, close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector: ESD sensitivity rating of the SIM interface pins is 1 kV (HBM), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device.
- Limit capacitance and series resistance on each SIM signal to match the SIM requirements (26.2 ns is the maximum allowed rise time on clock line, 1.0 μs is the maximum allowed rise time on data and reset lines).

![Figure 52: Application circuit for the connection to a single removable SIM card, with SIM detection implemented](image)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2, C3, C4</td>
<td>47 pF Capacitor Ceramic C0G 0402 5% 50 V</td>
<td>GRM1555C1H470JA01 - Murata</td>
</tr>
<tr>
<td>C5</td>
<td>100 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R71C104KA01 - Murata</td>
</tr>
<tr>
<td>D1, …, D6</td>
<td>Very Low Capacitance ESD Protection</td>
<td>PESD0402-140 - Tyco Electronics</td>
</tr>
<tr>
<td>R1</td>
<td>1 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-071KL - Yageo Phycomp</td>
</tr>
<tr>
<td>R2</td>
<td>470 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-07470KL - Yageo Phycomp</td>
</tr>
<tr>
<td>J1</td>
<td>SIM Card Holder, 6 + 2 p, with card presence switch</td>
<td>Various manufacturers, as CCM03-3013LFT R102 - C&amp;K</td>
</tr>
</tbody>
</table>

Table 38: Example of components for the connection to a single removable SIM card, with SIM detection implemented
Guidelines for dual SIM card / chip connection

Two SIM card / chip can be connected to the SIM interface of TOBY-L2 and MPCI-L2 series modules as described in the application circuits of Figure 53.

TOBY-L2 and MPCI-L2 series modules do not support the usage of two SIM at the same time, but two SIM can be populated on the application board, providing a proper switch to connect only the first or only the second SIM at a time to the SIM interface of the modules, as described in Figure 53.

TOBY-L2 modules “00”, “01” and “60” product versions and MPCI-L2 modules do not support SIM hot insertion / removal functionality, to enable / disable SIM interface upon detection of external SIM card physical insertion / removal: the physical connection between the external SIM and the module has to be provided before the module boot and then held for normal operation. Switching from one SIM to another can only be properly done within one of these two time periods:

- after TOBY-L2 module switch-off by the AT+CPWROFF and before TOBY-L2 module switch-on by PWR_ON
- after TOBY-L2 / MPCI-L2 module deregistration from network by AT+COPS=2 or by AT+CFUN=4 and before TOBY-L2 / MPCI-L2 module reset (reboot) by AT+CFUN=16 or AT+CFUN=1,1

TOBY-L2 modules (except “00”, “01” and “60” product versions) support SIM hot insertion / removal on the GPIO5 pin: if the feature is enabled using the specific AT commands (see sections 1.8.2 and 1.11, and u-blox AT Commands Manual [3], +UGPIOC, +UDCONF=50 commands), the switch from first SIM to the second SIM can be properly done when a Low logic level is present on the GPIO5 pin (“SIM not inserted” = SIM interface not enabled), without the necessity of a module re-boot, so that the SIM interface will be re-enabled by the module to use the second SIM when a high logic level is re-applied on the GPIO5 pin.

In the application circuit example represented in Figure 53, the application processor will drive the SIM switch using its own GPIO to properly select the SIM that is used by the module. Another GPIO may be used to handle the SIM hot insertion / removal function of TOBY-L2 modules, which can also be handled by other external circuits or by the cellular module GPIO according to the application requirements.

The dual SIM connection circuit described in Figure 53 can be implemented for SIM chips as well, providing proper connection between SIM chip and SIM interface as described in Figure 51.

If it is required to switch between more than 2 SIM, a circuit similar to the one described in Figure 53 can be implemented: in case of 4 SIM circuit, using proper 4-way switch instead of the suggested 2-way switches.

Follow these guidelines to connect the module to two external SIM connectors:

- Use a proper low on resistance (i.e. few ohms) and low on capacitance (i.e. few pF) 2-way analog switch (e.g. Fairchild FSA2567) as SIM switch to ensure high-speed data transfer according to SIM requirements.
- Connect the contacts C1 (VCC) and C6 (VPP) of the two UICC / SIM to the VSIM / UIM_PWR pin of the module by means of a proper 2-way analog switch (e.g. Fairchild FSA2567).
- Connect the contact C7 (VIO) of the two UICC / SIM to the SIM_IO / UIM_DATA pin of the module by means of a proper 2-way analog switch (e.g. Fairchild FSA2567).
- Connect the contact C3 (CLK) of the two UICC / SIM to the SIM_CLK / UIM_CLK pin of the module by means of a proper 2-way analog switch (e.g. Fairchild FSA2567).
- Connect the contact C2 (RST) of the two UICC / SIM to the SIM_RST / UIM_RESET pin of the module by means of a proper 2-way analog switch (e.g. Fairchild FSA2567).
- Connect the contact C5 (GND) of the two UICC / SIM to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply (VSIM / UIM_PWR), close to the related pad of the two SIM connectors, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, very close to each related pad of the two SIM connectors, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holders.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each pad of the two SIM connectors, according to the EMC/ESD requirements of the custom application.
• Limit capacitance and series resistance on each SIM signal to match the SIM requirements (26.2 ns is the maximum allowed rise time on clock line, 1.0 µs is the maximum allowed rise time on data and reset lines).

Figure 53: Application circuit for the connection to two removable SIM cards, with SIM detection not implemented

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number – Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1 – C4, C6 – C9</td>
<td>33 pF Capacitor Ceramic C0G 0402 5% 25 V</td>
<td>GRM1555C1H330JZ01 – Murata</td>
</tr>
<tr>
<td>C5, C10, C11</td>
<td>100 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R71C104KA01 – Murata</td>
</tr>
<tr>
<td>D1 – D8</td>
<td>Very Low Capacitance ESD Protection</td>
<td>PESD0402-140 - Tyco Electronics</td>
</tr>
<tr>
<td>R1</td>
<td>47 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-0747KL - Yageo Phycomp</td>
</tr>
<tr>
<td>J1, J2</td>
<td>SIM Card Holder, 6 + 2 p., with card presence switch</td>
<td>CCM03-3013LFT R102 - C&amp;K Components</td>
</tr>
<tr>
<td>U1</td>
<td>4PDT Analog Switch, with Low On-Capacitance and Low On-Resistance</td>
<td>FSA2567 - Fairchild Semiconductor</td>
</tr>
</tbody>
</table>

Table 39: Example of components for the connection to two removable SIM cards, with SIM detection not implemented
2.5.2 **Guidelines for SIM layout design**

The layout of the SIM card interface lines (VSIM, SIM_CLK, SIM_IO, SIM_RST or UIM_PWR, UIM_DATA, UIM_CLK, UIM_RESET) may be critical if the SIM card is placed far away from the TOBY-L2 and MPCI-L2 series modules or in close proximity to the RF antenna: these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface. It is recommended to keep the traces short and avoid coupling with RF line or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of LTE/3G/2G receiver channels whose carrier frequency is coincidental with harmonic frequencies. It is strongly recommended to place the RF bypass capacitors suggested in Figure 50 near the SIM connector.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges. Add adequate ESD protection as suggested to protect module SIM pins near the SIM connector.

Limit capacitance and series resistance on each SIM signal to match the SIM specifications. The connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.
2.6 Data communication interfaces

2.6.1 Universal Serial Bus (USB)

2.6.1.1 Guidelines for USB circuit design

The USB_D+ and USB_D- lines carry the USB serial data and signaling. The lines are used in single ended mode for full speed signaling handshake, as well as in differential mode for high speed signaling and data transfer.

USB pull-up or pull-down resistors and external series resistors on USB_D+ and USB_D- lines as required by the USB 2.0 specification [7] are part of the module USB pin driver and do not need to be externally provided.

- **VUSB_DET** functionality is not supported by all the TOBY-L2 series modules product versions: the pin should be left unconnected or it should not be driven high (for more details, see section 1.9.1.1).
- **VUSB_DET** pin is not available on MPCI-L2 series modules.

Routing the USB pins to a connector, they will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device with very low capacitance should be provided close to accessible point on the line connected to this pin, as described in Figure 54 and Table 40.

The USB interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. Tyco Electronics PESD0402-140 ESD protection device) on the lines connected to these pins, close to accessible points.

The USB_D+ and USB_D- pins of the modules can be directly connected to the USB host application processor without additional ESD protections if they are not externally accessible or according to EMC/ESD requirements.

![USB Interface application circuits](image)

**Figure 54: USB Interface application circuits**

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1, D2</td>
<td>Very Low Capacitance ESD Protection</td>
<td>PESD0402-140 - Tyco Electronics</td>
</tr>
</tbody>
</table>

**Table 40: Component for USB application circuits**

- If the USB interface pins are not used, they can be left unconnected on the application board, but it is recommended providing accessible test points directly connected to USB_D+ and USB_D- pins.
2.6.1.2 Guidelines for USB layout design

The USB_D+ / USB_D- lines require accurate layout design to achieve reliable signaling at the high speed data rate (up to 480 Mb/s) supported by the USB serial interface.

The characteristic impedance of the USB_D+ / USB_D- lines is specified by the Universal Serial Bus Revision 2.0 specification [7]. The most important parameter is the differential characteristic impedance applicable for the odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential. Signal integrity may be degraded if PCB layout is not optimal, especially when the USB signaling lines are very long.

Use the following general routing guidelines to minimize signal quality problems:

- Route USB_D+ / USB_D- lines as a differential pair
- Route USB_D+ / USB_D- lines as short as possible
- Ensure the differential characteristic impedance \( Z_{\text{diff}} \) is as close as possible to 90 Ω
- Ensure the common mode characteristic impedance \( Z_{\text{CM}} \) is as close as possible to 30 Ω
- Consider design rules for USB_D+ / USB_D- similar to RF transmission lines, being them coupled differential micro-strip or buried stripline: avoid any stubs, abrupt change of layout, and route on clear PCB area

Figure 55 and Figure 56 provide two examples of coplanar waveguide designs with differential characteristic impedance close to 90 Ω and common mode characteristic impedance close to 30 Ω. The first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

Figure 55: Example of USB line design, with \( Z_{\text{diff}} \) close to 90 Ω and \( Z_{\text{CM}} \) close to 30 Ω, for the described 4-layer board layup

Figure 56: Example of USB line design, with \( Z_{\text{diff}} \) close to 90 Ω and \( Z_{\text{CM}} \) close to 30 Ω, for the described 2-layer board layup
2.6.2  Asynchronous serial interface (UART)

The UART interface is not available on MPCI-L2 series modules.

2.6.2.1  Guidelines for UART circuit design

The UART interface is not supported by TOBY-L2 modules “00” product versions: all the UART pins should not be driven by any external device.

Providing the full RS-232 functionality (using the complete V.24 link)

If RS-232 compatible signal levels are needed, two different external voltage translators can be used to provide full RS-232 (9 lines) functionality: e.g. using the Texas Instruments SN74AVC8T245PW for the translation from 1.8 V to 3.3 V, and the Maxim MAX3237E for the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V Application Processor (DTE) is used and complete RS-232 functionality is required, then the complete 1.8 V UART interface of the module (DCE) should be connected to a 1.8 V DTE, as described in Figure 57.

![Figure 57: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8V DTE)](image)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module V_INTE output as 1.8 V supply for the voltage translators on the module side, as described in Figure 58.

![Figure 58: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)](image)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2, C3, C4</td>
<td>100 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R61A104KA01 - Murata</td>
</tr>
<tr>
<td>U1, U2</td>
<td>Unidirectional Voltage Translator</td>
<td>SN74AVC4T77419 - Texas Instruments</td>
</tr>
</tbody>
</table>

Table 41: Component for UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

19 Voltage translator providing partial power down feature so that the DTE 3.0 V supply can be also ramped up before V_INTE 1.8 V supply.
Providing the TXD, RXD, RTS and CTS lines only (not using the complete V.24 link)

If the functionality of the DSR, DCD, RI and DTR lines is not required in, or the lines are not available:

- Connect the module DTR input line to GND using a 0 Ω series resistor, since the module requires DTR active
- Leave DSR, DCD and RI lines of the module unconnected and floating

If RS-232 compatible signal levels are needed, the Maxim 13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V Application Processor is used, the circuit should be implemented as described in Figure 59.

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module V_INT output as 1.8 V supply for the voltage translators on the module side, as described in Figure 60.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2</td>
<td>100 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R61A104KA01 - Murata</td>
</tr>
<tr>
<td>U1</td>
<td>Unidirectional Voltage Translator</td>
<td>SN74AVC4T77420 - Texas Instruments</td>
</tr>
</tbody>
</table>

Table 42: Component for UART application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

20 Voltage translator providing partial power down feature so that the DTE 3.0 V supply can be also ramped up before V_INT 1.8 V supply
Providing the TXD and RXD lines only (not using the complete V24 link)

If the functionality of the CTS, RTS, DSR, DCD, RI and DTR lines is not required in the application, or the lines are not available, then:

- Connect the module RTS input line to GND or to the CTS output line of the module: since the module requires RTS active (low electrical level) if HW flow-control is enabled (AT&K3, that is the default setting), the pin can be connected using a 0 Ω series resistor to GND or to the active-module CTS (low electrical level) when the module is in active-mode, the UART interface is enabled and the HW flow-control is enabled
- Connect the module DTR input line to GND using a 0 Ω series resistor, as the module requires DTR active
- Leave DSR, DCD and RI lines of the module unconnected and floating

If RS-232 compatible signal levels are needed, the Maxim 13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V Application Processor (DTE) is used, the circuit that should be implemented as described in Figure 61.

![Figure 61: UART interface application circuit with partial V.24 link (3-wire) in the DTE/DCE serial communication (1.8V DTE)](image)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module V_INT output as 1.8 V supply for the voltage translators on the module side, as described in Figure 62.

![Figure 62: UART interface application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)](image)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2</td>
<td>100 nF Capacitor Ceramic X7R 0402 10% 16 V</td>
<td>GRM155R61A104KA01 - Murata</td>
</tr>
<tr>
<td>U1</td>
<td>Unidirectional Voltage Translator</td>
<td>SN74AVC2T245 - Texas Instruments</td>
</tr>
</tbody>
</table>

Table 43: Component for UART application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

---

11 Voltage translator providing partial power down feature so that the DTE 3.0 V supply can be also ramped up before V_INT 1.8 V supply
Additional considerations

If a 3.0 V Application Processor (DTE) is used, the voltage scaling from any 3.0 V output of the DTE to the corresponding 1.8 V input of the module (DCE) can be implemented as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-up integrated at the input of the module (DCE) for the correct selection of the voltage divider resistance values and mind that any DTE signal connected to the module must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the V_INT supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module (see the remark below).

Moreover, the voltage scaling from any 1.8 V output of the cellular module (DCE) to the corresponding 3.0 V input of the Application Processor (DTE) can be implemented by means of an appropriate low-cost non-inverting buffer with open drain output. The non-inverting buffer should be supplied by the V_INT supply output of the cellular module. Consider the value of the pull-up integrated at each input of the DTE (if any) and the baud rate required by the application for the appropriate selection of the resistance value for the external pull-up biased by the application processor supply rail.

If power saving is enabled the application circuit with the TXD and RXD lines only is not recommended. During command mode the DTE must send to the module a wake-up character or a dummy “AT” before each command line (see section 1.9.2.4 for the complete description), but during data mode the wake-up character or the dummy “AT” would affect the data communication.

Do not apply voltage to any UART interface pin before the switch-on of the UART supply source (V_INT), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance before V_INT switch-on.

ESD sensitivity rating of UART interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

If the UART interface pins are not used, they can be left unconnected on the application board, but it is recommended providing accessible test points directly connected to all the UART pins (TXD, RXD, RTS, CTS, DTR, DSR, DCD, RI) for diagnostic purpose, in particular providing a 0 Ω series jumper on each line to detach each UART pin of the module from the DTE application processor.

2.6.2.2 Guidelines for UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.
2.6.3 DDC (I²C) interface

The I²C bus compatible Display Data Channel interface is not available on MPCI-L2 series modules.

2.6.3.1 Guidelines for DDC (I²C) circuit design

I²C bus function is not supported by TOBY-L2 series modules “00”, “01”, “60” and TOBY-L201-02S product versions: the pins should not be driven by any external device.

The DDC I²C-bus master interface can be used to communicate with external I²C-bus slaves as an audio codec. Beside the general considerations reported below, see the section 2.7.1 for an application circuit example with an external audio codec I²C-bus slave.

To be compliant with the I²C bus specifications, the module bus interface pads are open drain output and pull up resistors must be mounted externally. Resistor values must conform to I²C bus specifications [13]: for example, 4.7 kΩ resistors can be commonly used. Pull-ups must be connected to a supply voltage of 1.8 V (typical), since this is the voltage domain of the DDC pins which are not tolerant to higher voltage values (e.g. 3.0 V).

Connect the DDC (I²C) pull-ups to the V_INT 1.8 V supply source, or another 1.8 V supply source enabled after V_INT, as any external signal connected to the DDC (I²C) interface must not be set high before the switch-on of the V_INT supply of DDC (I²C) pins, to avoid latch-up of circuits and let a proper boot of the module.

The signal shape is defined by the values of the pull-up resistors and the bus capacitance. Long wires on the bus will increase the capacitance. If the bus capacitance is increased, use pull-up resistors with nominal resistance value lower than 4.7 kΩ, to match the I²C bus specifications [13] regarding rise and fall times of the signals.

Capacitance and series resistance must be limited on the bus to match the I²C specifications (1.0 µs is the maximum allowed rise time on the SCL and SDA lines): route connections as short as possible.

If the pins are not used as DDC bus interface, they can be left unconnected.

ESD sensitivity rating of the DDC (I²C) pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

2.6.3.2 Guidelines for DDC (I²C) layout design

The DDC (I²C) serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.
2.6.4 Secure Digital Input Output interface (SDIO)

The SDIO Secure Digital Input Output interface is not available on MPCI-L2 series modules.

2.6.4.1 Guidelines for SDIO circuit design

The functionality of the SDIO Secure Digital Input Output interface pins is not supported by TOBY-L2 modules “00”, “01” and “60” product versions: the pins should not be driven by any external device.

TOBY-L2 series modules include a 4-bit Secure Digital Input Output interface (SDIO_D0, SDIO_D1, SDIO_D2, SDIO_D3, SDIO_CLK, SDIO_CMD) designed to communicate with an external u-blox short range Wi-Fi module.

Combining a u-blox cellular module with a u-blox short range communication module gives designers full access to the Wi-Fi module directly via the cellular module, so that a second interface connected to the Wi-Fi module is not necessary. AT commands via the AT interfaces of the cellular module (UART, USB) allows full control of the Wi-Fi module from any host processor, because Wi-Fi control messages are relayed to the Wi-Fi module via the dedicated SDIO interface (for more details, see the Wi-Fi AT commands in the u-blox AT Commands Manual [3] and see the Wi-Fi / Cellular Integration Application Note [15]).

Figure 63 and Table 44 show an application circuit for connecting TOBY-L2 series cellular modules (except “00”, “01” and “60” product versions) to u-blox ELLA-W131 short range Wi-Fi 802.11 b/g/n modules:

- The SDIO pins of the cellular module are connected to the related SDIO pins of the u-blox ELLA-W1 series short range Wi-Fi module, with appropriate low value series damping resistors to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.

  The most appropriate value for the series damping resistors on the SDIO lines depends on the specific line lengths and layout implemented. In general, the SDIO series resistors are not strictly required, but it is recommended to slow the SDIO signal, for example with 22 Ω or 33 Ω resistors, and avoid any possible ringing problem without violating the rise / fall time requirements.

- The V_INT supply output pin of the cellular module is connected to the shutdown input pin (SHDNn) of the two LDO regulators providing the 3.3 V and 1.8 V supply rails for the u-blox ELLA-W1 series Wi-Fi module, with appropriate pull-down resistors to avoid an improper switch on of the Wi-Fi module before the switch-on of the V_INT supply source of the cellular module SDIO interface pins.

- The GPIO1 pin of the cellular module is connected to the active low full power down input pin (PDn) of the u-blox ELLA-W1 series Wi-Fi module, implementing the Wi-Fi enable function.

- The configuration pin (CFG) of the u-blox ELLA-W1 series Wi-Fi module is connected to ground by means of a proper pull-down resistor for operation without sleep clock.

  The sleep clock input pin (SLEEP_CLK) of the u-blox ELLA-W1 series Wi-Fi module is left not connected, because an external clock source is not required.

- The WLAN LED open drain output pin (LED_0) of the u-blox ELLA-W1 series Wi-Fi module is connected to an LED with appropriate current limiting resistor, indicating Wi-Fi activity as additional optional feature.

- The WLAN antenna RF input/output (ANT1) of the u-blox ELLA-W131 Wi-Fi module is connected to a Wi-Fi antenna with an appropriate series Wi-Fi 2.4 GHz band-pass filter specifically designed for the coexistence between the Wi-Fi 2.4 GHz RF signals (2402...2482 MHz) and the LTE band 7 RF signals (2500...2690 MHz), as for example the Wi-Fi BAW 2.4 GHz band-pass filter TDK EPCOS B9604, or the TriQuint 885071, or the TriQuint 885032 or the Avago ACPF-7424, or the Taiyo Yuden F6HF2G441AF46.

- All GND pins of the cellular module and the u-blox ELLA-W1 series Wi-Fi module are connected to ground.

- All the other pins of the u-blox ELLA-W1 series Wi-Fi module are intended to be not connected.
Do not apply voltage to any SDIO interface pin before the switch-on of SDIO interface supply source (V_INT), to avoid latch-up of circuits and allow a proper boot of the module.

ESD sensitivity rating of SDIO interface pins is 1 kV (HMB according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and can be achieved by mounting a very low capacitance ESD protection (e.g. Tyco Electronics PESD0402-140 ESD), close to accessible points.

If the SDIO interface pins are not used, they can be left unconnected on the application board.

### 2.6.4.2 Guidelines for SDIO layout design

The SDIO serial interface requires the same consideration regarding electro-magnetic interference as any other high speed digital interface.

Keep the traces short, avoid stubs and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

Consider the usage of low value series damping resistors (see the application circuit in Figure 63 / Table 44) to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.
2.7 Audio interface

2.7.1 Digital audio interface

The I²S interface is not available on MPCI-L2 series modules.

2.7.1.1 Guidelines for digital audio circuit design

The I²S interface is not supported by TOBY-L2 series modules “00”, “01”, “60”, TOBY-L201-02S and TOBY-L220-62S product versions: the pins should not be driven by any external device.

I²S digital audio interface can be connected to an external digital audio device for voice applications. Any external digital audio device compliant with the configuration of the digital audio interface of the TOBY-L2 cellular module can be used, given that the external digital audio device must provide:

- The slave role: opposite role of TOBY-L2 modules, which act as master only
- The same mode and frame format: PCM / short synch mode or Normal I²S / long synch mode with
  - data in 2’s complement notation
  - MSB transmitted first
  - data word length = 16-bit (16 clock cycles)
  - frame length = synch signal period = 32-bit (32 clock cycles)
- The same sample rate, i.e. synch signal frequency, configurable by AT+UI2S <I²S_sample_rate> parameter
  - 8 kHz
  - 16 kHz
- The same serial clock frequency:
  - 32 x <I²S_sample_rate>
- Compatible voltage levels (1.80 V typ.), otherwise it is recommended to connect the 1.8 V digital audio interface of the module to the external 3.0 V (or similar) digital audio device by means of appropriate unidirectional voltage translators (e.g. TI SN74AVC4T774 or SN74AVC2T245, providing partial power down feature so that the digital audio device 3.0 V supply can be also ramped up before V_INT 1.8 V supply), using the module V_INT output as 1.8 V supply for the voltage translators on the module side
- Support of the side-tone, which is not available in the internal audio processing system of TOBY-L2 modules as summarized in Figure 26. The side-tone is a part of the user’s speech on uplink path that should be listened on downlink path by the user himself to have perception the call is on.

For the appropriate selection of a compliant external digital audio device, see section 1.10.1 and see the +UI2S AT command description in the u-blox AT Commands Manual [3] for further details regarding the capabilities and the possible settings of I²S digital audio interface of TOBY-L2 modules.

An appropriate specific application circuit has to be implemented and configured according to the particular external digital audio device or audio codec used and according to the application requirements.

Examples of manufacturers offering compatible audio codec parts are the following:

- Maxim Integrated (as the MAX9860, MAX9867, MAX9880A audio codecs)
- Texas Instruments / National Semiconductor
- Cirrus Logic / Wolfson Microelectronics
- Nuvoton Technology
- Asahi Kasei Microdevices
- Realtek Semiconductor
Figure 64 and Table 45 describe an application circuit for the i²S digital audio interface providing basic voice capability using an external audio voice codec, in particular the Maxim MAX9860 audio codec.

- DAC and ADC integrated in the external audio codec respectively converts an incoming digital data stream to analog audio output through a mono amplifier and converts the microphone input signal to the digital bit stream over the digital audio interface,
- A digital side-tone mixer integrated in the external audio codec provides loopback of the microphones/ADC signal to the DAC/headphone output.
- The module’s i²S interface (i²S master) is connected to the related pins of the external audio codec (i²S slave).
- The GPIO6 of the TOBY-L2 series module (that provides a suitable digital output clock) is connected to the clock input of the external audio codec to provide clock reference.
- The external audio codec is controlled by the TOBY-L2 series module using the DDC (i²C) interface, which can concurrently communicate with other i²C devices and control an external audio codec.
- The V_INT output supplies the external audio codec, defining proper digital interfaces voltage level.
- Additional components are provided for EMC and ESD immunity conformity: a 10 nF bypass capacitor and a series chip ferrite bead noise/EMI suppression filter provided on each microphone line input and speaker line output of the external codec as described in Figure 64 and Table 45. The necessity of these or other additional parts for EMC improvement may depend on the specific application board design.

Specific AT commands are available to configure the Maxim MAX9860 audio codec: for more details see the u-blox AT Commands Manual [3], +UVGC, +UEXTDCONF AT commands.

As various external audio codecs other than the one described in Figure 64 / Table 45 can be used to provide voice capability, the appropriate specific application circuit has to be implemented and configured according to the particular external digital audio device or audio codec used and according to the application requirements.

Figure 64: i²S interface application circuit with an external audio codec to provide voice capability
### Table 45: Example of components for audio voice codec application circuit

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number – Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>100 nF Capacitor Ceramic X5R 0402 10% 10V</td>
<td>GRM155R71C104KA01 – Murata</td>
</tr>
<tr>
<td>C2, C4, C5, C6</td>
<td>1 μF Capacitor Ceramic X5R 0402 10% 6.3 V</td>
<td>GRM155R60J105KE19 – Murata</td>
</tr>
<tr>
<td>C3</td>
<td>10 μF Capacitor Ceramic X5R 0603 20% 6.3 V</td>
<td>GRM188R60J106ME47 – Murata</td>
</tr>
<tr>
<td>C7, C8, C9, C10</td>
<td>27 pF Capacitor Ceramic COG 0402 5% 25 V</td>
<td>GRM1555C1H270JZ01 – Murata</td>
</tr>
<tr>
<td>C11, C12, C13, C14</td>
<td>10 nF Capacitor Ceramic X5R 0402 10% 50V</td>
<td>GRM155R71C103KA88 – Murata</td>
</tr>
<tr>
<td>D1, D2</td>
<td>Low Capacitance ESD Protection</td>
<td>USB0002RP or USB0002DP – AVX</td>
</tr>
<tr>
<td>EMI1, EMI2, EMI3, EMI4</td>
<td>Chip Ferrite Bead Noise/EMI Suppression Filter 1800 Ohm at 100 MHz, 2700 Ohm at 1 GHz</td>
<td>BLM15HD182SN1 – Murata</td>
</tr>
<tr>
<td>J1</td>
<td>Microphone Connector</td>
<td>Various manufacturers</td>
</tr>
<tr>
<td>J2</td>
<td>Speaker Connector</td>
<td>Various manufacturers</td>
</tr>
<tr>
<td>MIC</td>
<td>2.2 kΩ Electret Microphone</td>
<td>Various manufacturers</td>
</tr>
<tr>
<td>R1, R2</td>
<td>4.7 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-074K7L - Yageo Phycomp</td>
</tr>
<tr>
<td>R3</td>
<td>10 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-0710KL - Yageo Phycomp</td>
</tr>
<tr>
<td>R4, R5</td>
<td>2.2 kΩ Resistor 0402 5% 0.1 W</td>
<td>RC0402JR-072K2L – Yageo Phycomp</td>
</tr>
<tr>
<td>SPK</td>
<td>32 Ω Speaker</td>
<td>Various manufacturers</td>
</tr>
<tr>
<td>U1</td>
<td>16-Bit Mono Audio Voice Codec</td>
<td>MAX9860ETG+ - Maxim</td>
</tr>
</tbody>
</table>

Do not apply voltage to any I²S pin before the switch-on of I²S supply source (V_INT), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance before V_INT switch-on.

ESD sensitivity rating of I²S interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a general purpose ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

If the I²S digital audio pins are not used, they can be left unconnected on the application board.

#### 2.7.1.2 Guidelines for digital audio layout design

I²S interface and clock output lines require the same consideration regarding electro-magnetic interference as any other high speed digital interface. Keep the traces short and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

#### 2.7.1.3 Guidelines for analog audio layout design

Accurate design of the analog audio circuit is very important to obtain clear and high quality audio. The GSM signal burst has a repetition rate of 217 Hz that lies in the audible range. A careful layout is required to reduce the risk of noise from audio lines due to both VCC burst noise coupling and RF detection.

General guidelines for the uplink path (microphone), which is commonly the most sensitive, are the following:

- Avoid coupling of any noisy signal to microphone lines: it is strongly recommended to route microphone lines away from module VCC supply line, any switching regulator line, RF antenna lines, digital lines and any other possible noise source.
- Avoid coupling between microphone and speaker / receiver lines.
- Optimize the mechanical design of the application device, the position, orientation and mechanical fixing (for example, using rubber gaskets) of microphone and speaker parts in order to avoid echo interference between uplink path and downlink path.
- Keep ground separation from microphone lines to other noisy signals. Use an intermediate ground layer or vias wall for coplanar signals.
- In case of external audio device providing differential microphone input, route microphone signal lines as a differential pair embedded in ground to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise.
- Cross other signals lines on adjacent layers with 90° crossing.
- Place bypass capacitor for RF very close to active microphone. The preferred microphone should be designed for GSM applications which typically have internal built-in bypass capacitor for RF very close to active device. If the integrated FET detects the RF burst, the resulting DC level will be in the pass-band of the audio circuitry and cannot be filtered by any other device.

General guidelines for the downlink path (speaker / receiver) are the following:
- The physical width of the audio output lines on the application board must be wide enough to minimize series resistance since the lines are connected to low impedance speaker transducer.
- Avoid coupling of any noisy signal to speaker lines: it is recommended to route speaker lines away from module VCC supply line, any switching regulator line, RF antenna lines, digital lines and any other possible noise source.
- Avoid coupling between speaker / receiver and microphone lines.
- Optimize the mechanical design of the application device, the position, orientation and mechanical fixing (for example, using rubber gaskets) of speaker and microphone parts in order to avoid echo interference between downlink path and uplink path.
- In case of external audio device providing differential speaker / receiver output, route speaker signal lines as a differential pair embedded in ground up to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise.
- Cross other signals lines on adjacent layers with 90° crossing.
- Place bypass capacitor for RF close to the speaker.
2.8  General Purpose Input/Output

GPIOs are not supported by TOBY-L2 modules “00”, “01” and “60” product versions, except for the Wireless Wide Area Network status indication configured on the GPIO1: the pins should not be driven by any external device.

GPIOs are not available on MPCI-L2 series modules.

2.8.1.1  Guidelines for TOBY-L2 series GPIO circuit design

A typical usage of TOBY-L2 modules’ GPIOs can be the following:

- Network indication provided over GPIO1 or GPIO4 pin (see Figure 65 / Table 46 below)
- Wi-Fi enable provided over GPIO4 or GPIO1 pin (see Figure 63 / Table 44 in section 2.6.4)
- SIM card detection provided over GPIO5 (see Figure 52 / Table 38 or Figure 53 / Table 39 in section 2.5)
- Clock output provided over GPIO6 (see Figure 64 / Table 45 in section 2.7.1)

![Figure 65: Application circuit for network indication provided over GPIO1](image)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Part Number - Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>10 kΩ Resistor 0402 5% 0.1 W</td>
<td>Various manufacturers</td>
</tr>
<tr>
<td>R2</td>
<td>47 kΩ Resistor 0402 5% 0.1 W</td>
<td>Various manufacturers</td>
</tr>
<tr>
<td>R3</td>
<td>820 Ω Resistor 0402 5% 0.1 W</td>
<td>Various manufacturers</td>
</tr>
<tr>
<td>DL1</td>
<td>LED Red SMT 0603</td>
<td>LTST-C190KRKT - Lite-on Technology Corporation</td>
</tr>
<tr>
<td>T1</td>
<td>NPN BJT Transistor</td>
<td>BC847 - Infineon</td>
</tr>
</tbody>
</table>

Table 46: Components for network indication application circuit

Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO of TOBY-L2 modules.

Do not apply voltage to any GPIO of TOBY-L2 before the switch-on of the GPIOs supply (V_INT), to avoid latch-up of circuits and allow a proper module boot. If the external signals connected to the module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. T1 SN74CB3Q16244, TSSA3159, TSSA63157) between the two-circuit connections and set to high impedance before V_INT switch-on.

ESD sensitivity rating of the GPIO pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

If the GPIO pins are not used, they can be left unconnected on the application board.

2.8.1.2  Guidelines for general purpose input/output layout design

The general purpose inputs / outputs pins are generally not critical for layout.
2.9 Mini PCIe specific signals (W_DISABLE#, LED_WWAN#)

Mini PCI Express specific signals (W_DISABLE#, LED_WWAN#) are not available on TOBY-L2 series.

2.9.1.1 Guidelines for W_DISABLE# circuit design

As described in Figure 66, the MPCI-L2 series modules W_DISABLE# wireless disable input is equipped with an internal pull-up to the 3.3Vaux supply: an external pull-up resistor is not required and should not be provided. If connecting the W_DISABLE# input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device should be provided close to accessible point, as described in Figure 66 and Table 47.

ESD sensitivity rating of the W_DISABLE# pin is 1 kV (HBM according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the W_DISABLE# pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible point.

An open drain output is suitable to drive the W_DISABLE# input from an application processor as it is equipped with an internal pull-up to the 3.3Vaux supply as described in Figure 66. A compatible push-pull output of an application processor can also be used. In any case, take care to set the proper level in all the possible scenarios to avoid an inappropriate disabling of the radio operations.

![Figure 66: W_DISABLE# application circuit using a push button and an open drain output of an application processor](image)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD</td>
<td>Varistor for ESD protection</td>
<td>CT0402S14AHSG - EPCOS</td>
</tr>
</tbody>
</table>

Table 47: Example of ESD protection component for the W_DISABLE# application circuit

If the W_DISABLE# functionality is not required by the application, the pin can be left unconnected.
2.9.1.2 Guidelines for LED_WWAN# circuit design

As described in Figure 67 and Table 48, the MPCI-L2 series modules LED_WWAN# active-low open drain output can be directly connected to a system-mounted LED to provide the Wireless Wide Area Network status indication as specified by the PCI Express Mini Card Electromechanical Specification [16].

![Diagram of LED_WWAN# application circuit](image)

Figure 67: LED_WWAN# application circuit

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>DL</td>
<td>LED Green SMT 0603</td>
<td>LTST-C190KGKT - Lite-on Technology Corporation</td>
</tr>
<tr>
<td>R</td>
<td>470 Ω Resistor 0402 5% 0.1 W</td>
<td>Various manufacturers</td>
</tr>
</tbody>
</table>

Table 48: Example of components for the LED_WWAN# application circuit

- ESD sensitivity rating of the LED_WWAN# pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the line is externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible point.
- If the LED_WWAN# functionality is not required by the application, the pin can be left unconnected.

2.9.1.3 Guidelines for W_DISABLE# and LED_WWAN# layout design

The W_DISABLE# and LED_WWAN# circuits are generally not critical for layout.

2.10 Reserved pins (RSVD)

Pins reserved for future use, marked as RSVD, are not available on MPCI-L2 series.

TOBY-L2 series modules have pins reserved for future use. All the RSVD pins are to be left unconnected on the application board except the RSVD pin number 6 which must be connected to ground as described in Figure 68.

![Diagram of application circuit for the reserved pins (RSVD)](image)

Figure 68: Application circuit for the reserved pins (RSVD)
2.11 Module placement

An optimized placement allows a minimum RF line’s length and closer path from DC source for VCC / 3.3Vaux. Make sure that the module, analog parts and RF circuits are clearly separated from any possible source of radiated energy. In particular, digital circuits can radiate digital frequency harmonics, which can produce Electro-Magnetic Interference that affects the module, analog parts and RF circuits’ performance. Implement proper countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Make sure that the module, RF and analog parts / circuits, and high speed digital circuits are clearly separated from any sensitive part / circuit which may be affected by Electro-Magnetic Interference, or employ countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Provide enough clearance between the module and any external part.

The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application base-board below the TOBY-L2 and MPCI-L2 series modules: avoid placing temperature sensitive devices close to the module.
2.12 TOBY-L2 series module footprint and paste mask

Figure 69 and Table 49 describe the suggested footprint (i.e. copper mask) layout for TOBY-L2 series modules. The proposed land pattern layout slightly reflects the modules’ pads layout, with most of the lateral pads designed wider on the application board (1.8 x 0.8 mm) than on the module (1.5 x 0.8 mm).

The Non Solder Mask Defined (NSMD) pad type is recommended over the Solder Mask Defined (SMD) pad type, implementing the solder mask opening 50 µm larger per side than the corresponding copper pad.

The suggested paste mask layout for TOBY-L2 series modules slightly reflects the copper mask layout described in Figure 69 and Table 49, as different stencil apertures layout for any specific pad is recommended:

- Blue marked pads: Paste layout reduced circumferentially about 0.025 mm to Copper layout
- Green marked pads: Paste layout enlarged circumferentially about 0.025 mm to Copper layout
- Purple marked pads: Paste layout one to one to Copper layout

The recommended solder paste thickness is 150 µm, according to application production process requirements.

These are recommendations only and not specifications. The exact mask geometries, distances and stencil thicknesses must be adapted to the specific production processes (e.g. soldering etc.) of the customer.
2.13 MPCI-L2 series module installation

MPCI-L2 series modules are fully compliant with the 52-pin PCI Express Full-Mini Card Type F2 form factor, i.e., top-side and bottom-side keep-out areas, 50.95 mm nominal length, 30 mm nominal width, and all the other dimensions as defined by the PCI Express Mini Card Electromechanical Specification [16], except for the card thickness (which nominal value is 3.7 mm), as described in Figure 70.

![Figure 70: MPCI-L2 series mechanical description (top, side and bottom views)](image)

MPCI-L2 series modules are fully compliant with the 52-pin PCI Express Full-Mini card edge type system connector as defined by the PCI Express Mini Card Electromechanical Specification [16]. Table 50 describes some examples of 52-pin mating system connectors for the MPCI-L2 series PCI Express Full-Mini card modules.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>JAE Electronics</td>
<td>MM60 series</td>
<td>52-circuit, 0.8 mm pitch, PCI Express Mini card edge female connector</td>
</tr>
<tr>
<td>Molex</td>
<td>67910 series</td>
<td>52-circuit, 0.8 mm pitch, PCI Express Mini card edge female connector</td>
</tr>
<tr>
<td>TE Connectivity / AMP</td>
<td>2041119 series</td>
<td>52-circuit, 0.8 mm pitch, PCI Express Mini card edge female connector</td>
</tr>
<tr>
<td>FCI</td>
<td>10123824 series</td>
<td>52-circuit, 0.8 mm pitch, PCI Express Mini card edge female connector</td>
</tr>
</tbody>
</table>

Table 50: MPCI-L2 series PCI Express Full-Mini card compatible connector

- It is recommended to use the two mounting holes described in Figure 70 to fix (ground) the MPCI-L2 module to the main ground of the application board with suitable screws and fasteners.
- Follow the recommendations provided by the connector manufacturer and the guidelines available in the PCI Express Mini Card Electromechanical Specification [16] for the development of the footprint (i.e. the copper mask) PCB layout for the mating edge system connector. The exact geometries, distances and stencil thicknesses should be adapted to the specific production processes (e.g. soldering etc.).
- Follow the recommendations provided by the connector manufacturer to properly insert and remove the MPCI-L2 series modules.
MPCI-L2 series modules are equipped with two Hirose U.FL-R-SMT RF receptacles for ANT1 / ANT2 ports, which require a suitable mated RF plug from the same connector series as the examples listed in Table 31.

To mate the connectors, the mating axes of both connectors must be aligned. The "click" will confirm the fully mated connection. Do not attempt to insert on an extreme angle: insert the RF plug connectors vertically into the ANT1 / ANT2 RF receptacles of the modules, as described in Figure 71.

**Figure 71: Precautions during RF connector mating**

To unplug the RF cable assembly it is encouraged to use a suitable extraction tool for the RF connector, such as the Hirose U.FL-LP-N or the Hirose U.FL-LP(V)-N extraction jig, according to the RF cable assembly type used.

Hook the end portion of the extraction jig onto the connector cover and pull off vertically in the direction of the connector mating axis, as described in Figure 72.

**Figure 72: Precautions during RF connector extraction**

Any attempt to unplug the RF connectors by pulling on the cable assembly without using a suitable extraction tool may result in damage and affect the RF performance. Do not forcefully twist, deform, or apply any excessive pull force to the RF cables or damage the RF connectors, otherwise the RF performance may be reduced.
2.14 Thermal guidelines

Modules' operating temperature range is specified in TOBY-L2 Data Sheet [1] and MPCI-L2 Data Sheet [2].

The most critical condition concerning module thermal performance is the uplink transmission at maximum power (data upload in connected-mode), when the baseband processor runs at full speed, radio circuits are all active and the RF power amplifier is driven to higher output RF power. This scenario is not often encountered in real networks (for example, see the Terminal Tx Power distribution for WCDMA, taken from operation on a live network, described in the GSMA TS.09 Battery Life Measurement and Current Consumption Technique [17]); however the application should be correctly designed to cope with it.

During transmission at maximum RF power the TOBY-L2 and MPCI-L2 series modules generate thermal power that may exceed 3 W: this is an indicative value since the exact generated power strictly depends on operating condition such as the actual antenna return loss, the number of allocated TX resource blocks, the transmitting frequency band, etc. The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application.

The spreading of the Module-to-Ambient thermal resistance (Rth,M-A) depends on the module operating condition. The overall temperature distribution is influenced by the configuration of the active components during the specific mode of operation and their different thermal resistance toward the case interface.

The Module-to-Ambient thermal resistance value and the relative increase of module temperature will differ according to the specific mechanical deployments of the module, e.g. application PCB with different dimensions and characteristics, mechanical shells enclosure, or forced air flow.

The increase of the thermal dissipation, i.e. the reduction of the Module-to-Ambient thermal resistance, will decrease the temperature of the modules' internal circuitry for a given operating ambient temperature. This improves the device long-term reliability in particular for applications operating at high ambient temperature.

Recommended hardware techniques to be used to improve heat dissipation in the application:

- Connect each GND pin with solid ground layer of the application board and connect each ground area of the multilayer application board with complete thermal via stacked down to main ground layer.
- Use the two mounting holes described in Figure 70 to fix (ground) the MPCI-L2 modules to the main ground of the application board with suitable screws and fasteners.
- Provide a ground plane as wide as possible on the application board.
- Optimize antenna return loss, to optimize overall electrical performance of the module including a decrease of module thermal power.
- Optimize the thermal design of any high-power components included in the application, such as linear regulators and amplifiers, to optimize overall temperature distribution in the application device.
- Select the material, the thickness and the surface of the box (i.e. the mechanical enclosure) of the application device that integrates the module so that it provides good thermal dissipation.
- Follow the thermal guidelines for integrating wireless wide area network mini card add-in cards, such as the MPCI-L2 series modules, as provided in the PCI Express Mini Card Electromechanical Specification [16].

Further hardware techniques that may be considered to improve the heat dissipation in the application:

- Force ventilation air-flow within mechanical enclosure.
- Provide a heat sink component attached to the module top side, with electrically insulated / high thermal conductivity adhesive, or on the backside of the application board, below the cellular module, as a large part of the heat is transported through the GND pads of the TOBY-L2 series LGA modules and dissipated over the backside of the application board.
For example, the Module-to-Ambient thermal resistance ($R_{th,M-A}$) is strongly reduced with forced air ventilation and a heat-sink installed on the back of the application board, decreasing the module temperature variation. Beside the reduction of the Module-to-Ambient thermal resistance implemented by proper application hardware design, the increase of module temperature can be moderated by proper application software implementation:

- Enable power saving configuration using the AT+UPSV command (see section 1.15.16).
- Enable module connected-mode for a given time period and then disable it for a time period enough long to properly mitigate temperature increase.

2.15 ESD guidelines

The sections 2.15.1 and 2.15.2 are related to EMC / ESD immunity. The modules are ESD sensitive devices. The ESD sensitivity for each pin (as Human Body Model according to JESD22-A114F) is specified in TOBY-L2 series Data Sheet [1] or MPCI-L2 series Data Sheet [2]. Special precautions are required when handling the pins; for ESD handling guidelines see section 3.2.

2.15.1 ESD immunity test overview

The immunity of devices integrating TOBY-L2 and MPCI-L2 series modules to Electro-Static Discharge (ESD) is part of the Electro-Magnetic Compatibility (EMC) conformity which is required for products bearing the CE marking, compliant with the Radio Equipment Directive (2014/53/EU), the EMC Directive (2014/30/EU) and the Low Voltage Directive (2014/35/EU) issued by the Commission of the European Community.

Compliance with these directives implies conformity to the following European Norms for device ESD immunity: ESD testing standard CENELEC EN 61000-4-2 [18] and the radio equipment standards ETSI EN 301 489-1 [19], ETSI EN 301 489-52 [20], which requirements are summarized in Table 51.

The ESD immunity test is performed at the enclosure port, defined by ETSI EN 301 489-1 [19] as the physical boundary through which the electromagnetic field radiates. If the device implements an integral antenna, the enclosure port is seen as all insulating and conductive surfaces housing the device. If the device implements a removable antenna, the antenna port can be separated from the enclosure port. The antenna port includes the antenna element and its interconnecting cable surfaces.

The applicability of ESD immunity test to the whole device depends on the device classification as defined by ETSI EN 301 489-1 [19]. Applicability of ESD immunity test to the relative device ports or the relative interconnecting cables to auxiliary equipment, depends on device accessible interfaces and manufacturer requirements, as defined by ETSI EN 301 489-1 [19].

Contact discharges are performed at conductive surfaces, while air discharges are performed at insulating surfaces. Indirect contact discharges are performed on the measurement setup horizontal and vertical coupling planes as defined in CENELEC EN 61000-4-2 [18].

For the definition of integral antenna, removable antenna, antenna port and device classification see ETSI EN 301 489-1 [19]. For the contact / air discharges definitions see CENELEC EN 61000-4-2 [18].

<table>
<thead>
<tr>
<th>Application</th>
<th>Category</th>
<th>Immunity Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration</td>
<td>Contact Discharge</td>
<td>4 kV</td>
</tr>
<tr>
<td></td>
<td>Air Discharge</td>
<td>8 kV</td>
</tr>
</tbody>
</table>

Table 51: EMC / ESD immunity requirements as defined by CENELEC EN 61000-4-2 and ETSI EN 301 489-1, ETSI EN 301 489-52
2.15.2 ESD immunity test of TOBY-L2 and MPCI-L2 series reference designs

Although EMC / ESD certification is required for customized devices integrating TOBY-L2 and MPCI-L2 series modules for European Conformance CE mark, EMC certification (including ESD immunity) has been successfully performed on TOBY-L2 and MPCI-L2 series modules reference design according to European Norms summarized in Table 51.

The EMC / ESD approved u-blox reference designs consist of a TOBY-L2 and MPCI-L2 series module installed onto a motherboard which provides supply interface, SIM card and communication port. External LTE/3G/2G antennas are connected to the provided connectors.

Since external antennas are used, the antenna port can be separated from the enclosure port. The reference design is not enclosed in a box so that the enclosure port is not identified with physical surfaces. Therefore, some test cases cannot be applied. Only the antenna port is identified as accessible for direct ESD exposure.

Table 52 reports the u-blox TOBY-L2 and MPCI-L2 series reference designs ESD immunity test results, according to test requirements stated in CENELEC EN 61000-4-2 [18], ETSI EN 301 489-1 [19], ETSI EN 301 489-52 [20].

<table>
<thead>
<tr>
<th>Category</th>
<th>Application</th>
<th>Immunity Level</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contact Discharge to coupling planes (indirect contact discharge)</td>
<td>Enclosure</td>
<td>±4 kV / -4 kV</td>
<td></td>
</tr>
<tr>
<td>Contact Discharges to conducted surfaces (direct contact discharge)</td>
<td>Enclosure port</td>
<td>Not Applicable</td>
<td>Test not applicable to u-blox reference design because it does not provide enclosure surface. The test is applicable only to equipment providing conductive enclosure surface.</td>
</tr>
<tr>
<td></td>
<td>Antenna ports</td>
<td>±4 kV / -4 kV</td>
<td>Test applicable to u-blox reference design because it provides antennas with conductive &amp; insulating surfaces. The test is applicable only to equipment providing antennas with conductive surface.</td>
</tr>
<tr>
<td>Air Discharge at insulating surfaces</td>
<td>Enclosure port</td>
<td>Not Applicable</td>
<td>Test not applicable to the u-blox reference design because it does not provide an enclosure surface. The test is applicable only to equipment providing insulating enclosure surface.</td>
</tr>
<tr>
<td></td>
<td>Antenna ports</td>
<td>±8 kV / -8 kV</td>
<td>Test applicable to u-blox reference design because it provides antennas with conductive &amp; insulating surfaces. The test is applicable only to equipment providing antennas with insulating surface.</td>
</tr>
</tbody>
</table>

Table 52: Enclosure ESD immunity level of u-blox TOBY-L2 and MPCI-L2 series modules reference designs

TOBY-L2 and MPCI-L2 reference design implement all the ESD precautions described in section 2.15.3.

2.15.3 ESD application circuits

The application circuits described in this section are recommended and should be implemented in the device integrating TOBY-L2 and MPCI-L2 series modules, according to the application device classification (see ETSI EN 301 489-1 [19]), to satisfy the requirements for ESD immunity test summarized in Table 51.

Antenna interface

The ANT1 and ANT2 ports of TOBY-L2 and MPCI-L2 series modules provide ESD immunity up to ±4 kV for direct Contact Discharge and up to ±8 kV for Air Discharge: no further precaution to ESD immunity test is needed, as implemented in the EMC / ESD approved reference design of TOBY-L2 and MPCI-L2 series modules.
The antenna interface application circuit implemented in the EMC / ESD approved reference designs of TOBY-L2 and MPCI-L2 series modules is described in Figure 48 in case of antennas detection circuit not implemented, and is described in Figure 49 and Table 35 in case of antennas detection circuit implemented (section 2.4).

**RESET_N and PERST# pin**

The following precautions are suggested for the **RESET_N** and the **PERST#** line of TOBY-L2 and MPCI-L2 series modules, depending on the application board handling, to satisfy ESD immunity test requirements:

- It is recommended to keep the connection line to **RESET_N** and **PERST#** as short as possible

Maximum ESD sensitivity rating of the **RESET_N** and the **PERST#** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the **RESET_N** or **PERST#** pin is externally accessible on the application board. The following precautions are suggested to achieve higher protection level:

- A general purpose ESD protection device (e.g. EPCOS CA05P4S14THSG varistor array or EPCOS CT0402S14AHSG varistor) should be mounted on the **RESET_N** or **PERST#** line, close to accessible point

The **RESET_N** and **PERST#** application circuit implemented in the EMC / ESD approved reference designs of TOBY-L2 and MPCI-L2 series modules is described in Figure 43 and Table 30 (section 2.3.2).

**SIM interface**

The following precautions are suggested for TOBY-L2 and MPCI-L2 series modules SIM interface, depending on the application board handling, to satisfy ESD immunity test requirements:

- A bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) must be mounted on the lines connected to the SIM interface pins to assure SIM interface functionality when an electrostatic discharge is applied to the application board enclosure

- It is suggested to use as short as possible connection lines at SIM pins

Maximum ESD sensitivity rating of SIM interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if SIM interface pins are externally accessible on the application board. The following precautions are suggested to achieve higher protection level:

- A low capacitance (i.e. less than 10 pF) ESD protection device (e.g. Tyco Electronics PESD0402-140) should be mounted on each SIM interface line, close to accessible points (i.e. close to the SIM card holder)

The SIM interface application circuit implemented in the EMC / ESD approved reference designs of TOBY-L2 and MPCI-L2 series modules is described in Figure 50 and Table 36 (section 2.5).

**Other pins and interfaces**

All the module pins that are externally accessible on the device integrating TOBY-L2 and MPCI-L2 series module should be included in the ESD immunity test since they are considered to be a port as defined in ETSI EN 301 489-1 [19]. Depending on applicability, to satisfy ESD immunity test requirements according to ESD category level, all the module pins that are externally accessible should be protected up to ±4 kV for direct Contact Discharge and up to ±8 kV for Air Discharge applied to the enclosure surface.

The maximum ESD sensitivity rating of all the other pins of the module is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the relative pin is externally accessible on the application board. The following precautions are suggested to achieve higher protection level:

- **USB interface**: a very low capacitance (i.e. less or equal to 1 pF) ESD protection device (e.g. Tyco Electronics PESD0402-140 ESD protection device) should be mounted on the **USB_D+** and **USB_D-** lines, close to the accessible points (i.e. close to the USB connector)

- **Other pins**: a general purpose ESD protection device (e.g. EPCOS CA05P4S14THSG varistor array or EPCOS CT0402S14AHSG varistor) should be mounted on the related line, close to accessible point
2.16 Schematic for TOBY-L2 and MPCI-L2 series module integration

2.16.1 Schematic for TOBY-L2 module “00” product version

Figure 73 is an example of a schematic diagram where a TOBY-L2 cellular module “00” product version is integrated into an application board, using all the available interfaces and functions of the module.

Figure 73: Example of schematic diagram to integrate a TOBY-L200-00S or TOBY-L210-00S in an application, using all interfaces.
### 2.16.2 Schematic for TOBY-L2 module “01” or “60” product versions

Figure 74 is an example of a schematic diagram where a TOBY-L2 cellular module “01” or “60” product version is integrated into an application board, using all the available interfaces and functions of the module.

![Schematic diagram](image-url)
2.16.3 Schematic for TOBY-L2 module “02”, “03” or “62” product versions

Figure 75 is an example of a schematic diagram where a TOBY-L2 cellular module “02”, “03” or “62” product version is integrated into an application board, using all the available interfaces and functions of the module.

Figure 75: Example schematic diagram: integrating TOBY-L2 module ‘02’, ‘03’ or ‘62’ version in an application using all interfaces
2.16.4 Schematic for MPCI-L2 series

Figure 76 is an example of a schematic diagram where a MPCI-L2 series module is integrated into an application board, using all the available interfaces and functions of the module.

Figure 76: Example of schematic diagram to integrate a MPCI-L2 series module in an application board, using all the interfaces
2.17 Design-in checklist

This section provides a design-in checklist.

2.17.1 Schematic checklist

The following are the most important points for a simple schematic check:

- DC supply must provide a nominal voltage at **VCC / 3.3Vaux** pin within the operating range limits.
- DC supply must be capable of supporting both the highest peak and the highest averaged current consumption values in connected-mode, as specified in the TOBY-L2 series Data Sheet [1] or in the MPCI-L2 series Data Sheet [2].
- **VCC / 3.3Vaux** voltage supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.
- Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- Check that voltage level of any connected pin does not exceed the relative operating range.
- Check **USB_D+ / USB_D-** signal lines as well as very low capacitance ESD protections if accessible.
- Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- Insert the suggested capacitors on each SIM signal and low capacitance ESD protections if accessible.
- Check UART signals direction, as the TOBY-L2 signal names follow the ITU-T V.24 Recommendation [8].
- Consider providing appropriate low value series damping resistors on SDIO lines to avoid reflections.
- Add a proper pull-up resistor (e.g. 4.7 kΩ) to **V_INT** or another proper 1.8 V supply on each DDC (I²C) interface line, if the interface is used.
- Check the digital audio interface specifications to connect a proper external audio device.
- Consider passive filtering parts on each used analog audio line.
- Provide accessible test points directly connected to the following pins of the TOBY-L2 series modules: **V_INT, PWR_ON**, and **RESET_N** for diagnostic purpose.
- Provide accessible test points directly connected to all the UART pins of the TOBY-L2 series modules (**TXD, RXD, RTS, CTS, DTR, DSR, DCD, RI**) for diagnostic purpose, in particular providing a 0 Ω series jumper on each line to detach each UART pin of the module from the DTE application processor.
- If the USB is not used, provide accessible test points directly connected to the **USB_D+** and **USB_D-** pins.
- Provide proper precautions for EMC / ESD immunity as required on the application board.
- Do not apply voltage to any generic digital interface pin of TOBY-L2 series modules before the switch-on of the generic digital interface supply source (**V_INT**).
- All unused pins can be left unconnected except the **RSVD** pin number 6 of TOBY-L2 series modules, which must be connected to GND.
### 2.17.2 Layout checklist

The following are the most important points for a simple layout check:

- **Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the ANT1 and the ANT2 ports (antenna RF interfaces).**
- **Ensure no coupling occurs between the RF interface and noisy or sensitive signals (primarily analog audio input/output signals, SIM signals, high-speed digital lines such as SDIO, USB and other data lines).**
- **Optimize placement for minimum length of RF line.**
- **Check the footprint and paste mask designed for TOBY-L2 module as illustrated in section 2.12.**
- **VCC / 3.3Vaux line should be wide and as short as possible.**
- **Route VCC / 3.3Vaux supply line away from RF lines / parts and other sensitive analog lines / parts.**
- **The VCC / 3.3Vaux bypass capacitors in the picoFarad range should be placed as close as possible to the VCC / 3.3Vaux pins, in particular if the application device integrates an internal antenna.**
- **Ensure an optimal grounding connecting each GND pin with application board solid ground layer.**
- **Use as many vias as possible to connect the ground planes on multilayer application board, providing a dense line of vias at the edges of each ground area, in particular along RF and high speed lines.**
- **Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.**
- **USB_D+ / USB_D- traces should meet the characteristic impedance requirement (90 Ω differential and 30 Ω common mode) and should not be routed close to any RF line / part.**
- **Keep the SDIO traces short, avoid stubs, avoid coupling with any RF line / part and consider low value series damping resistors to avoid reflections and other losses in signal integrity.**
- **Ensure appropriate RF precautions for the Wi-Fi and Cellular technologies coexistence as described in section 2.6.4 and in the Wi-Fi / Cellular Integration Application Note [15].**
- **Ensure appropriate RF precautions for the GNSS and Cellular technologies coexistence as described in the GNSS Implementation Application Note [14].**
- **Route analog audio signals away from noisy sources (primarily RF interface, VCC, switching supplies).**
- **The audio outputs lines on the application board must be wide enough to minimize series resistance.**

### 2.17.3 Antenna checklist

- **Antenna termination should provide 50 Ω characteristic impedance with V.S.W.R at least less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.**
- **Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).**
- **Ensure compliance with any regulatory agency RF radiation requirement, as reported in sections 4.2.2 and/or 4.3.1 for products marked with the FCC and/or IC.**
- **Ensure high and similar efficiency for both the primary (ANT1) and the secondary (ANT2) antenna.**
- **Ensure high isolation between the primary (ANT1) and the secondary (ANT2) antenna.**
- **Ensure low Envelope Correlation Coefficient between the primary (ANT1) and the secondary (ANT2) antenna: the 3D antenna radiation patterns should have radiation lobes in different directions.**
- **Ensure high isolation between the cellular antennas and any other antenna or transmitter.**
3 Handling and soldering

No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to TOBY-L2 series reels / tapes, MPCI-L2 series trays, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning, see the TOBY-L2 series Data Sheet [1], the MPCI-L2 series Data Sheet [2] and the u-blox Package Information Guide [27].

3.2 Handling

The TOBY-L2 and MPCI-L2 series modules are Electro-Static Discharge (ESD) sensitive devices. Ensure ESD precautions are implemented during handling of the module.

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of TOBY-L2 and MPCI-L2 series modules (as Human Body Model according to JESD22-A114F) is specified in the TOBY-L2 series Data Sheet [1] or the MPCI-L2 series Data Sheet [2].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the TOBY-L2 and MPCI-L2 series modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron,…).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD safe soldering iron.

For more robust designs, employ additional ESD protection measures on the application device integrating the TOBY-L2 and MPCI-L2 series modules, as described in section 2.15.3.
3.3 Soldering

3.3.1 Soldering paste

“No Clean” soldering paste is strongly recommended for TOBY-L2 series modules, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

- **Soldering Paste:** OM338 SAC405 / Nr.143714 (Cookson Electronics)
- **Alloy specification:** 95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper)
- **Alloy specification:** 95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
- **Melting Temperature:** 217 °C
- **Stencil Thickness:** 150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures. The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.12.

The quality of the solder joints on the connectors (“half vias”) should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type-soldering oven is strongly recommended for TOBY-L2 series modules over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.


Reflow profiles are to be selected according to the following recommendations.

**Failure to observe these recommendations can result in severe damage to the device!**

**Preheat phase**
Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- **Temperature rise rate:** max 3 °C/s  
  If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- **Time:** 60 – 120 s  
  If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- **End Temperature:** 150 - 200 °C  
  If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

**Heating/ reflow phase**
The temperature rises above the liquidus temperature of 217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- **Limit time above 217 °C liquidus temperature:** 40 - 60 s  
  **Peak reflow temperature:** 245 °C

**Cooling phase**
A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- **Temperature fall rate:** max 4 °C/s
To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

**Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.**

![Recommended Soldering Profile](image)

*Figure 77: Recommended soldering profile*

The modules must not be soldered with a damp heat process.

### 3.3.3 Optical inspection

After soldering the TOBY-L2 series modules, inspect the modules optically to verify that the module is properly aligned and centered.

### 3.3.4 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results use a “no clean” soldering paste and eliminate the cleaning step after the soldering.
3.3.5  Repeated reflow soldering
Only a single reflow soldering process is encouraged for boards with a module populated on it.

3.3.6  Wave soldering
Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with the modules.

3.3.7  Hand soldering
Hand soldering is not recommended.

3.3.8  Rework
Rework is not recommended.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9  Conformal coating
Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products. These materials affect the HF properties of the cellular modules and it is important to prevent them from flowing into the module.
The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

Conformal Coating of the module will void the warranty.

3.3.10  Casting
If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the cellular modules before implementing this in the production.

Casting will void the warranty.

3.3.11  Grounding metal covers
Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

u-blox gives no warranty for damages to the cellular modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12  Use of ultrasonic processes
The cellular modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the module.

u-blox gives no warranty against damages to the cellular modules caused by any Ultrasonic Processes.
4 Approvals

For the complete list and details regarding all the certification schemes approvals of TOBY-L2 and MPCI-L2 series modules, see the TOBY-L2 Data Sheet [1] and the MPCI-L2 Data Sheet [2], or visit our website (www.u-blox.com), or please contact the u-blox office or sales representative nearest you.

4.1 Product certification approval overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called “certification schemes” that can be divided into three distinct categories:

- Regulatory certification
  - Country specific approval required by local government in most regions and countries, such as:
    - CE (Conformité Européenne) marking for European Union
    - FCC (Federal Communications Commission) approval for United States

- Industry certification
  - Telecom industry specific approval verifying the interoperability between devices and networks:
    - GCF (Global Certification Forum), partnership between European device manufacturers and network operators to ensure and verify global interoperability between devices and networks
    - PTCRB (PCS Type Certification Review Board), created by United States network operators to ensure and verify interoperability between devices and North America networks

- Operator certification
  - Operator specific approval required by some mobile network operator, such as:
    - AT&T network operator in United States

Even if TOBY-L2 and MPCI-L2 series modules are approved under all major certification schemes, the application device that integrates TOBY-L2 and MPCI-L2 series modules must be approved under all the certification schemes required by the specific application device to be deployed in the market. The required certification scheme approvals and relative testing specifications differ depending on the country or the region where the device that integrates TOBY-L2 and MPCI-L2 series modules must be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device must operate.

Check the appropriate applicability of the TOBY-L2 / MPCI-L2 module’s approvals while starting the certification process of the device integrating the module: the re-use of the u-blox cellular module’s approval can significantly reduce the cost and time to market of the application device certification.

The certification of the application device that integrates a TOBY-L2 module or a MPCI-L2 module and the compliance of the application device with all the applicable certification schemes, directives and standards are the sole responsibility of the application device manufacturer.

TOBY-L2 and MPCI-L2 series modules are certified according to all capabilities and options stated in the Protocol Implementation Conformance Statement document (PICS) of the module. The PICS, according to the 3GPP TS 51.010-2 [21], 3GPP TS 34.121-2 [22], 3GPP TS 36.521-2 [24] and 3GPP TS 36.523-2 [25], is a statement of the implemented and supported capabilities and options of a device.

The PICS document of the application device integrating TOBY-L2 and MPCI-L2 series modules must be updated from the module PICS statement if any feature stated as supported by the module in its PICS document is not implemented or disabled in the application device. For more details regarding the AT commands settings that affect the PICS, see the u-blox AT Commands Manual [3].

Check the specific settings required for mobile network operators approvals as they may differ from the AT commands settings defined in the module as integrated in the application device.
4.2 US Federal Communications Commission notice

United States Federal Communications Commission (FCC) IDs:

- u-blox TOBY-L200 cellular modules: XPYTOBYL200
- u-blox TOBY-L201 cellular modules: XPYTOBYL201
- u-blox TOBY-L210 cellular modules: XPYTOBYL210
- u-blox TOBY-L280 cellular modules: XPYTOBYL280
- u-blox MPCI-L200 cellular modules: Contains FCC ID XPYTOBYL200
- u-blox MPCI-L201 cellular modules: Contains FCC ID XPYTOBYL201
- u-blox MPCI-L210 cellular modules: Contains FCC ID XPYTOBYL210
- u-blox MPCI-L280 cellular modules: Contains FCC ID XPYTOBYL280

4.2.1 Safety warnings review the structure

- Equipment for building-in. The requirements for fire enclosure must be evaluated in the end product
- The clearance and creepage current distances required by the end product must be withheld when the module is installed
- The cooling of the end product shall not negatively be influenced by the installation of the module
- Excessive sound pressure from earphones and headphones can cause hearing loss
- No natural rubbers, hygroscopic materials, or materials containing asbestos are employed

4.2.2 Declaration of Conformity

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

The gain of the system antenna(s) used for the TOBY-L200, TOBY-L210, MPCI-L200, MPCI-L210 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 9.8 dBi (in 700 MHz, i.e. LTE FDD-17 band), 4.3 dBi (in 850 MHz, i.e. GSM 850 or UMTS FDD-5 or LTE FDD-5 band), 5.5 dBi (in 1700 MHz, i.e. AWS or UMTS FDD-4 or LTE FDD-4 band), 2.8 dBi (in 1900 MHz, i.e. GSM 1900 or UMTS FDD-2 or LTE FDD-2 band), 6.0 dBi (in 2500 MHz, i.e. LTE FDD-7 band) for mobile and fixed or mobile operating configurations.

The gain of the system antenna(s) used for TOBY-L201, MPCI-L201 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 9.8 dBi (700 MHz, i.e. LTE FDD-17 band), 10.2 dBi (750 MHz, i.e. LTE FDD-13 band), 10.0 dBi (850 MHz, i.e. UMTS FDD-5 or LTE FDD-5 band), 6.8 dBi (1700 MHz, i.e. AWS or LTE FDD-4 band), 8.5 dBi (1900 MHz, i.e. UMTS FDD-2 or LTE FDD-2 band) for mobile and fixed or mobile operating configurations.

The gain of the system antenna(s) used for TOBY-L280, MPCI-L280 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 4.3 dBi (850 MHz, i.e. GSM 850 or UMTS FDD-5 or LTE FDD-5 band), 3.4 dBi (1900 MHz, i.e. GSM 1900 or UMTS FDD-2 or LTE FDD-2 band), 10.8 dBi (2500 MHz, i.e. LTE FDD-7 band) for mobile and fixed or mobile operating configurations.
4.2.3 Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user’s authority to operate the equipment.

Manufacturers of mobile or fixed devices incorporating the TOBY-L2 and MPCI-L2 series modules are authorized to use the FCC Grants of the TOBY-L2 series modules for their own final products according to the conditions referenced in the certificates.

The FCC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:
"Contains FCC ID: XPYTOBYL200" resp.
"Contains FCC ID: XPYTOBYL201" resp.
"Contains FCC ID: XPYTOBYL210" resp.
"Contains FCC ID: XPYTOBYL280" resp.

IMPORTANT: Manufacturers of portable applications incorporating the TOBY-L2 and MPCI-L2 series modules are required to have their final product certified and apply for their own FCC Grant related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices. Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

Additional Note: as per 47CFR15.105 this equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
  o Reorient or relocate the receiving antenna
  o Increase the separation between the equipment and receiver
  o Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
  o Consult the dealer or an experienced radio/TV technician for help

4.3 Innovation, Science and Economic Development Canada notice

ISED Canada (formerly known as IC - Industry Canada) Certification Numbers:

- u-blox TOBY-L200 cellular modules: 8595A-TOBYL200
- u-blox TOBY-L201 cellular modules: 8595A-TOBYL201
- u-blox TOBY-L210 cellular modules: 8595A-TOBYL210
- u-blox TOBY-L280 cellular modules: 8595A-TOBYL280
- u-blox MPCI-L200 cellular modules: Contains IC 8595A-TOBYL200
- u-blox MPCI-L201 cellular modules: Contains IC 8595A-TOBYL201
- u-blox MPCI-L210 cellular modules: Contains IC 8595A-TOBYL210
- u-blox MPCI-L280 cellular modules: Contains IC 8595A-TOBYL280
4.3.1 Declaration of Conformity

Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

The gain of the system antenna(s) used for the TOBY-L200, TOBY-L210, MPCI-L200, MPCI-L210 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 9.8 dBi (700 MHz, i.e. LTE FDD-17 band), 4.3 dBi (850 MHz, i.e. GSM 850 or UMTS FDD-5 or LTE FDD-5 band), 5.5 dBi (1700 MHz, i.e. AWS or UMTS FDD-4 or LTE FDD-4 band), 2.8 dBi (1900 MHz, i.e. GSM 1900 or UMTS FDD-2 or LTE FDD-2 band), 6.0 dBi (2500 MHz, i.e. LTE FDD-7 band) for mobile and fixed or mobile operating configurations.

The gain of the system antenna(s) used for TOBY-L201, MPCI-L201 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 6.7 dBi (700 MHz, i.e. LTE FDD-17 band), 6.9 dBi (750 MHz, i.e. LTE FDD-13 band), 6.7 dBi (850 MHz, i.e. UMTS FDD-5 or LTE FDD-5 band), 6.8 dBi (1700 MHz, i.e. AWS or LTE FDD-4 band), 8.5 dBi (1900 MHz, i.e. UMTS FDD-2 or LTE FDD-2 band) for mobile and fixed or mobile operating configurations.

The gain of the system antenna(s) used for TOBY-L280, MPCI-L280 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 1.0 dBi (850 MHz, i.e. GSM 850 or UMTS FDD-5 or LTE FDD-5 band), 3.4 dBi (1900 MHz, i.e. GSM 1900 or UMTS FDD-2 or LTE FDD-2 band), 3.3 dBi (2500 MHz, i.e. LTE FDD-7 band) for mobile and fixed or mobile operating configurations.

4.3.2 Modifications

The ISED Canada requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user’s authority to operate the equipment.

Manufacturers of mobile or fixed devices incorporating the TOBY-L2 and MPCI-L2 series modules are authorized to use the ISED Canada Certificates of the TOBY-L2 series modules for their own final products according to the conditions referenced in the certificates.

The ISED Canada Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

"Contains IC: 8595A-TOBYL200" resp.
"Contains IC: 8595A-TOBYL201" resp.
"Contains IC: 8595A-TOBYL210" resp.
"Contains IC: 8595A-TOBYL280" resp.

Innovation, Science and Economic Development Canada (ISED) Notices

This Class B digital apparatus complies with Canadian CAN ICES-3(B) / NMB-3(B) and RSS-210.

Operation is subject to the following two conditions:

- this device may not cause interference
- this device must accept any interference, including interference that may cause undesired operation of the device
Radio Frequency (RF) Exposure Information

The radiated output power of the u-blox Cellular Module is below the Innovation, Science and Economic Development Canada (ISED) radio frequency exposure limits. The u-blox Cellular Module should be used in such a manner such that the potential for human contact during normal operation is minimized.

This device has been evaluated and shown compliant with the ISED RF Exposure limits under mobile exposure conditions (antennas are greater than 20 cm from a person's body).

This device has been approved for use in Canada. Status of the listing in the Innovation, Science and Economic Development's REL (Radio Equipment List) can be found at the following web address:


Additional Canadian information on RF exposure also can be found at the following web address: http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

IMPORTANT: Manufacturers of portable applications incorporating the TOBY-L2 and MPCI-L2 series modules are required to have their final product certified and apply for their own Innovation, Science and Economic Development Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

IMPORTANT: les fabricants d'applications portables contenant les modules TOBY-L2 et MPCI-L2 series doivent faire certifier leur produit final et déposer directement leur candidature pour une certification FCC ainsi que pour un certificat ISDE Canada délivré par l'organisme chargé de ce type d'appareil portable. Ceci est obligatoire afin d'être en accord avec les exigences SAR pour les appareils portables.

Tout changement ou modification non expressément approuvé par la partie responsable de la certification peut annuler le droit d'utiliser l'équipement.
4.4 Brazilian Anatel certification

TOBY-L200, MPCI-L200, TOBY-L280 and MPCI-L280 modules are certified by the Brazilian Agency of Telecommunications (Agência Nacional de Telecomunicações in Portuguese) (Anatel).

Anatel IDs for the TOBY-L200 modules:
- EAN barcode: (01)0 789 8941 57523 6
- Homologation number 00806-15-05903

Anatel IDs for the MPCI-L200 modules:
- EAN barcode: (01)0 789 8941 57524 3
- Homologation number 00806-15-05903

Anatel IDs for the TOBY-L280 modules:
- EAN barcode: (01)0 789 8941 57527 4
- Homologation number 04537-15-05903

Anatel IDs for the MPCI-L280 modules:
- EAN barcode: (01)0 789 8941 57528 1
- Homologation number: 04537-15-05903
4.5 European Conformance CE mark

The TOBY-L2 and MPCI-L2 series cellular modules (except TOBY-L201, MPCI-L201, TOBY-L220 and MPCI-L220) have been evaluated against the essential requirements of the 2014/53/EU Radio Equipment Directive.

In order to satisfy the essential requirements of the 2014/53/EU Radio Equipment Directive, the modules are compliant with the following standards:

- Radio Frequency spectrum use (Article 3.2):
  - EN 301 511 V12.5.1
  - EN 301 908-1 V11.1.1
  - EN 301 908-2 V11.1.1
  - EN 301 908-13 V11.1.1

- Electromagnetic Compatibility (Article 3.1b):
  - EN 301 489-1 V2.1.1
  - EN 301 489-52 V1.1.1

- Health and Safety (Article 3.1a)
  - EN 62311:2008

⚠️ Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

The conformity assessment procedure for the modules, referred to in Article 17 and detailed in Annex II of Directive 2014/53/EU has been followed.

Thus, the following marking is included in the product:

![CE]
### 4.6 Australian Regulatory Compliance Mark

TOBY-L210, MPCI-L210, TOBY-L280 and MPCI-L280 modules are compliant with the Standards made by the Australian Communications and Media Authority (ACMA) under Section 376 of the Telecommunications Act 1997.

Modules are compliant with the following list of standards:

- AS/CA S042.1-2011: Requirements for connection to an air interface of a Telecommunications Network - Part 1
- AS/ACIF S042.3-2005: Requirements for connection to an air interface of a Telecommunications Network - Part 3
- AS/CA S042.4-2011: Requirements for connection to an air interface of a Telecommunications Network - Part 4

### 4.7 Taiwanese NCC certification

TOBY-L210, MPCI-L210, TOBY-L280, and MPCI-L280 modules are certified by Taiwanese National Communications Commission (NCC), with the following NCC IDs:

- TOBY-L210: CCAI15Z10030T0
- MPCI-L210: CCAI15Z10050T6
- TOBY-L280: CCAI15Z10120T1
- MPCI-L280: CCAI15Z10190T9
4.8 Japanese Giteki certification

The following modules product versions are Giteki certified and have the Giteki mark placed on the label:

- **TOBY-L210-60S**
  - T: D150056003
  - R: 003-150062
- **TOBY-L210-62S**
  - T: ADF150154003
  - R: 003-150062
- **TOBY-L220**
  - T: AD160008003
  - R: 003-160019
- **MPCI-L210-60S**
  - T: D150057003
  - R: 003-150063
- **MPCI-L220**
  - T: AD160009003
  - R: 003-160020

![Figure 78: Label of TOBY-L210-60S, TOBY-L210-62S and TOBY-L220 modules product versions with Giteki mark](image1)

![Figure 79: Label of MPCI-L210-60S and MPCI-L220 modules product versions with Giteki mark](image2)
5 Product testing

5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested automatically in production line. Stringent quality control process has been implemented in the production line. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment (ATE) in production line, which logs all production and measurement data. A detailed test report for each unit can be generated from the system. Figure 80 illustrates typical automatic test equipment (ATE) in a production line.

The following typical tests are among the production tests.
- Digital self-test (firmware download, Flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (USB interface communication, SIM card communication)
- Digital tests (GPIOs and other interfaces)
- Measurement and calibration of RF characteristics in all supported bands (such as receiver S/N verification, frequency tuning of reference clock, calibration of transmitter and receiver power levels, etc.)
- Verification of RF characteristics after calibration (i.e. modulation accuracy, power levels, spectrum, etc. are checked to ensure they are all within tolerances when calibration parameters are applied)

Figure 80: Automatic test equipment for module tests
5.2 Test parameters for OEM manufacturer

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

However, an OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damage the module components
  - All module pins are well soldered on device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

Dedicated tests can be implemented to check the device. For example, the measurement of module current consumption when set in a specified status can detect a short circuit if compared with a “Golden Device” result.

In addition, module AT commands can be used to perform functional tests on digital interfaces (communication with host controller, check SIM interface, GPIOs, etc.), on audio interfaces (audio loop for test purposes can be enabled by the AT+UPAR=2 command as described in the u-blox AT Commands Manual [3]), and to perform RF performance tests (see the following section 5.2.2 for details).

5.2.1 “Go/No go” tests for integrated devices

A “Go/No go” test is typically to compare the signal quality with a “Golden Device” in a location with excellent network coverage and known signal quality. This test should be performed after data connection has been established. AT+CSQ is the typical AT command used to check signal quality in term of RSSI. See the u-blox AT Commands Manual [3] for detail usage of the AT command.

These kinds of test may be useful as a “go/no go” test but not for RF performance measurements.

This test is suitable to check the functionality of communication with host controller, SIM card as well as power supply. It is also a means to verify if components at antenna interface are well soldered.

5.2.2 RF functional tests

The overall RF functional test of the device including the antenna can be performed with basic instruments such as a spectrum analyzer (or an RF power meter) and a signal generator with the assistance of AT+UTEST command over AT command user interface.

The AT+UTEST command provides a simple interface to set the module to Rx or Tx test modes ignoring the LTE/3G/2G signaling protocol. The command can set the module into:

- transmitting mode in a specified channel and power level in all supported modulation schemes and bands
- receiving mode in a specified channel to returns the measured power level in all supported bands

See the u-blox AT Commands Manual [3] and the End user test Application Note [26], for the AT+UTEST command syntax description and detail guide of usage.
This feature allows the measurement of the transmitter and receiver power levels to check component assembly related to the module antenna interface and to check other device interfaces from which depends the RF performance.

- To avoid module damage during transmitter test, a proper antenna according to module specifications or a 50 Ω termination must be connected to ANT1 port.
- To avoid module damage during receiver test the maximum power level received at ANT1 and ANT2 ports must meet module specifications.

The AT+UTEST command sets the module to emit RF power ignoring LTE/3G/2G signaling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purpose in controlled environments by qualified user and must not be used during the normal module operation. Follow instructions suggested in u-blox documentation. u-blox assumes no responsibilities for the inappropriate use of this feature.

Figure 81 illustrates a typical test setup for such RF functional test.

![Test Setup Diagram](image)

**Figure 81:** Setup with spectrum analyzer or power meter and signal generator for radiated measurements
Appendix

A Migration between TOBY-L1 and TOBY-L2

A.1 Overview

TOBY-L1 and TOBY-L2 series cellular modules have exactly the same TOBY form factor (35.6 x 24.8 mm LGA) with exactly the same 152-pin layout as described in Figure 82, so that the modules can be alternatively mounted on a single application board using exactly the same copper mask, solder mask and paste mask.

Figure 82: TOBY-L1 and TOBY-L2 series modules pad layout and pin assignment

TOBY modules are also form-factor compatible with the u-blox LISA, SARA and LARA cellular module families: although TOBY modules, LISA modules (33.2 x 22.4 mm, 76-pin LCC), SARA modules (26.0 x 16.0 mm, 96-pin LGA) and LARA modules (26.0 x 24.0 mm, 100-pin LGA) each have different form factors, the footprints for the TOBY, LISA, SARA and LARA modules have been developed to ensure layout compatibility.

With the u-blox “nested design” solution, any TOBY, LISA, SARA or LARA module can be alternatively mounted on the same space of a single “nested” application board as described in Figure 83. Guidelines in order to implement a nested application board, description of the u-blox reference nested design and comparison between TOBY, LISA, SARA and LARA modules are provided in the Nested Design Application Note [28].

Figure 83: TOBY, LISA, SARA, LARA modules’ layout compatibility: all modules are accommodated on the same nested footprint
Table 53 summarizes the interfaces provided: TOBY-L2 series modules make available additional interfaces over pins remarked as reserved on TOBY-L1 series modules (highlighted in blue in Figure 82).

<table>
<thead>
<tr>
<th>Module</th>
<th>RF / Radio Access Technology</th>
<th>Power</th>
<th>System</th>
<th>SIM</th>
<th>Serial</th>
<th>Audio</th>
<th>GPIO</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOBY-L100</td>
<td>3, 4, 13</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>TOBY-L200</td>
<td>4, 2, 4, 5, 7, 17</td>
<td>24, 6</td>
<td>1, 2, 4, 5, 8, 12 Quad</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>TOBY-L201</td>
<td>4, 2, 4, 5, 13, 17</td>
<td>24, 6</td>
<td>2, 5</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>TOBY-L210</td>
<td>4, 1, 3, 5, 7, 8, 20</td>
<td>24, 6</td>
<td>1, 2, 5, 8, 12 Quad</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>TOBY-L220</td>
<td>4, 1, 3, 5, 8, 19</td>
<td>24, 6</td>
<td>1, 2, 5, 8, 12 Quad</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>TOBY-L280</td>
<td>4, 1, 3, 5, 7, 8, 28</td>
<td>24, 6</td>
<td>1, 2, 5, 8, 12 Quad</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
</tbody>
</table>

= supported by all product versions
= supported by all product versions except versions “00”, “60”
= supported by all product versions except version “00”
= supported by all product versions except versions “62”

Table 53: Summary of TOBY-L1 series and TOBY-L2 series modules interfaces

Figure 84 summarizes the LTE, 3G and 2G operating frequency bands of TOBY-L1 and TOBY-L2 series modules.

Figure 84: Summary of TOBY-L1 and TOBY-L2 series modules LTE, 3G and 2G operating frequency bands

3) TOBY-L220-62S product version does not support 3G Radio Access Technology
## A.2 Pin-out comparison between TOBY-L1 and TOBY-L2

<table>
<thead>
<tr>
<th>Pin No</th>
<th>TOBY-L1 Pin Name</th>
<th>Description</th>
<th>TOBY-L2 Pin Name</th>
<th>Description</th>
<th>Remarks for migration</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RSVD</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>V_BCKP</td>
<td>RTC Supply Output 2.5 V output only RTC backup function not available</td>
<td>V_BCKP</td>
<td>RTC Supply Input/Output 3.0 V output 1.4 V – 4.2 V input (RTC backup)</td>
<td>RTC back-up: No → Yes</td>
</tr>
<tr>
<td>4</td>
<td>RSVD</td>
<td>Reserved</td>
<td>VUSB_DET</td>
<td>VBUS USB supply (5 V) detection</td>
<td>No difference: leave unconnected as reserved or not supported</td>
</tr>
<tr>
<td>5</td>
<td>V_INT</td>
<td>Interfaces Supply Output 1.8 V output</td>
<td>V_INT</td>
<td>Interfaces Supply Output 1.8 V output</td>
<td>No functional difference</td>
</tr>
<tr>
<td>6</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RSVD</td>
<td>Reserved</td>
<td>This pin must be connected to GND No connect → Connect to GND</td>
</tr>
<tr>
<td>7-9</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RSVD</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>RSVD</td>
<td>Reserved</td>
<td>DSR</td>
<td>UART DSR Output2 / GPIO2</td>
<td>Reserved → UART / GPIO</td>
</tr>
<tr>
<td>11</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RI</td>
<td>UART RI Output2 / GPIO2</td>
<td>Reserved → UART / GPIO</td>
</tr>
<tr>
<td>12</td>
<td>RSVD</td>
<td>Reserved</td>
<td>DCD</td>
<td>UART DCD Output2 / GPIO2</td>
<td>Reserved → UART / GPIO</td>
</tr>
<tr>
<td>13</td>
<td>RSVD</td>
<td>Reserved</td>
<td>DTR</td>
<td>UART DTR Input2 / GPIO2</td>
<td>Reserved → UART / GPIO</td>
</tr>
<tr>
<td>14</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RTS</td>
<td>UART RTS Input2</td>
<td>Reserved → UART</td>
</tr>
<tr>
<td>15</td>
<td>RSVD</td>
<td>Reserved</td>
<td>CTS</td>
<td>UART CTS Output2</td>
<td>Reserved → UART</td>
</tr>
<tr>
<td>16</td>
<td>RSVD</td>
<td>Reserved</td>
<td>TXD</td>
<td>UART Data Input2</td>
<td>Reserved → UART</td>
</tr>
<tr>
<td>17</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RXD</td>
<td>UART Data Output2</td>
<td>Reserved → UART</td>
</tr>
<tr>
<td>18-19</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RSVD</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>PWIR_ON</td>
<td>Power-on Input No internal pull-up</td>
<td>PWIR_ON</td>
<td>Power-on Input Internal 50k pull-up to VCC</td>
<td>Pull-up: External → Internal</td>
</tr>
<tr>
<td>21</td>
<td>GPIO1</td>
<td>GPIO2 WWAN status indication on “00” product version</td>
<td>GPIO1</td>
<td>GPIO2 WWAN status indication on “00”, “01” and “60” product versions</td>
<td>No functional difference</td>
</tr>
<tr>
<td>22</td>
<td>GPIO2</td>
<td>GPIO2 WWAN status indication on “00” product version</td>
<td>GPIO2</td>
<td>GPIO2 WWAN status indication on “00”, “01” and “60” product versions</td>
<td>No functional difference</td>
</tr>
<tr>
<td>23</td>
<td>RESET_N</td>
<td>Reset signal Input Internal 10k pull-up to V_BCKP Switch-off function only</td>
<td>RESET_N</td>
<td>Reset signal Input Internal 50k pull-up to VCC Reset, Switch-on, Switch-off</td>
<td>Internal pull-up: V_BCKP → VCC Switch-off → Reset, Switch-on/off</td>
</tr>
<tr>
<td>24</td>
<td>GPIO3</td>
<td>GPIO3 WWAN status indication on “00” product version</td>
<td>GPIO3</td>
<td>GPIO3 WWAN status indication on “00”, “01” and “60” product versions</td>
<td>No functional difference</td>
</tr>
<tr>
<td>25</td>
<td>GPIO4</td>
<td>GPIO4 WWAN status indication on “00” product version</td>
<td>GPIO4</td>
<td>GPIO4 WWAN status indication on “00”, “01” and “60” product versions</td>
<td>No functional difference</td>
</tr>
<tr>
<td>26</td>
<td>RSVD</td>
<td>Reserved</td>
<td>HOST_SELECT0</td>
<td>Input for selection of module configuration by the host13</td>
<td>Reserved → HOST_SELECT0</td>
</tr>
<tr>
<td>27</td>
<td>USB_D-</td>
<td>USB Data I/O (D-)</td>
<td>USB_D-</td>
<td>USB Data I/O (D-)</td>
<td>No functional difference</td>
</tr>
<tr>
<td>28</td>
<td>USB_D+</td>
<td>USB Data I/O (D+)</td>
<td>USB_D+</td>
<td>USB Data I/O (D+)</td>
<td>No functional difference</td>
</tr>
<tr>
<td>29</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RSVD</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RSVD</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>33-43</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RSVD</td>
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<td></td>
</tr>
<tr>
<td>44</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RSVD</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>47-49</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RSVD</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>RSVD</td>
<td>Reserved</td>
<td>I2S_WA</td>
<td>I2S Word Alignment14 / GPIO15</td>
<td>Reserved → I2S / GPIO</td>
</tr>
<tr>
<td>51</td>
<td>RSVD</td>
<td>Reserved</td>
<td>I2S_TXD</td>
<td>I2S Data Output14 / GPIO15</td>
<td>Reserved → I2S / GPIO</td>
</tr>
<tr>
<td>52</td>
<td>RSVD</td>
<td>Reserved</td>
<td>I2S_CLK</td>
<td>I2S Clock14 / GPIO15</td>
<td>Reserved → I2S / GPIO</td>
</tr>
<tr>
<td>53</td>
<td>RSVD</td>
<td>Reserved</td>
<td>I2S_RXD</td>
<td>I2S Data Input14 / GPIO14</td>
<td>Reserved → I2S / GPIO</td>
</tr>
</tbody>
</table>

---

1 Not supported by all product versions 
2 Not supported by “00” product versions 
3 Not supported by “00”, “01”, “60” product versions 
4 Not supported by current product version 
5 Not supported by “00”, “01”, “60”, TOBY-L201-02S, TOBY-L220-62S product versions
<table>
<thead>
<tr>
<th>Pin No</th>
<th>TOBY-L1 Pin Name</th>
<th>Description</th>
<th>TOBY-L2 Pin Name</th>
<th>Description</th>
<th>Remarks for migration</th>
</tr>
</thead>
<tbody>
<tr>
<td>54</td>
<td>RSVD</td>
<td>Reserved</td>
<td>SCL</td>
<td>I2C Clock Output*</td>
<td>Reserved → I2C</td>
</tr>
<tr>
<td>55</td>
<td>RSVD</td>
<td>Reserved</td>
<td>SDA</td>
<td>I2C Data I/O*</td>
<td>Reserved → I2C</td>
</tr>
<tr>
<td>56</td>
<td>SIM_CLK</td>
<td>SIM Clock Output</td>
<td>SIM_CLK</td>
<td>SIM Clock Output</td>
<td>No functional difference</td>
</tr>
<tr>
<td>57</td>
<td>SIM_IO</td>
<td>SIM Data I/O</td>
<td>SIM_IO</td>
<td>SIM Data I/O</td>
<td>No functional difference</td>
</tr>
<tr>
<td>58</td>
<td>SIM_RST</td>
<td>SIM Reset Output</td>
<td>SIM_RST</td>
<td>SIM Reset Output</td>
<td>No functional difference</td>
</tr>
<tr>
<td>59</td>
<td>VSIM</td>
<td>SIM Supply Output</td>
<td>VSIM</td>
<td>SIM Supply Output</td>
<td>No functional difference</td>
</tr>
<tr>
<td>60</td>
<td>GPIO5</td>
<td>GPIO**</td>
<td>GPIO5</td>
<td>GPIO**</td>
<td>SIM detection</td>
</tr>
<tr>
<td>61</td>
<td>GPIO6</td>
<td>GPIO**</td>
<td>GPIO6</td>
<td>GPIO**</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>RSVD</td>
<td>Reserved</td>
<td>HOST_SELECT1</td>
<td>Input for selection of module configuration by the host**</td>
<td>Reserved → HOST_SELECT1</td>
</tr>
<tr>
<td>63</td>
<td>RSVD</td>
<td>Reserved</td>
<td>SDIO_D2</td>
<td>SDIO serial data [2]**</td>
<td>Reserved → SDIO</td>
</tr>
<tr>
<td>64</td>
<td>RSVD</td>
<td>Reserved</td>
<td>SDIO_CLK</td>
<td>SDIO serial clock**</td>
<td>Reserved → SDIO</td>
</tr>
<tr>
<td>65</td>
<td>RSVD</td>
<td>Reserved</td>
<td>SDIO_CMD</td>
<td>SDIO command**</td>
<td>Reserved → SDIO</td>
</tr>
<tr>
<td>66</td>
<td>RSVD</td>
<td>Reserved</td>
<td>SDIO_D0</td>
<td>SDIO serial data [0]**</td>
<td>Reserved → SDIO</td>
</tr>
<tr>
<td>67</td>
<td>RSVD</td>
<td>Reserved</td>
<td>SDIO_D3</td>
<td>SDIO serial data [3]**</td>
<td>Reserved → SDIO</td>
</tr>
<tr>
<td>68</td>
<td>RSVD</td>
<td>Reserved</td>
<td>SDIO_D1</td>
<td>SDIO serial data [1]**</td>
<td>Reserved → SDIO</td>
</tr>
<tr>
<td>69</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>70-72</td>
<td>VCC</td>
<td>Module Supply Input 3.40 V – 4.50 V normal range</td>
<td>VCC</td>
<td>Module Supply Input 3.40 V – 4.35 V normal range</td>
<td>No VCC functional difference</td>
</tr>
<tr>
<td>73-74</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>75</td>
<td>RSVD</td>
<td>Reserved</td>
<td>ANT_DET</td>
<td>Antenna Detection Input**</td>
<td>Reserved → ANT_DET</td>
</tr>
<tr>
<td>76</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>77</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RSVD</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>78-80</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>81</td>
<td>ANT1</td>
<td>RF Antenna Input/Output Two LTE bands</td>
<td>ANT1</td>
<td>RF Antenna Input/Output Up to six LTE bands</td>
<td>No RF functional difference Different operating bands support</td>
</tr>
<tr>
<td>82-83</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>84</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RSVD</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>85-86</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>87</td>
<td>ANT2</td>
<td>RF Antenna Input LTE MIMO 2x2</td>
<td>ANT2</td>
<td>RF Antenna Input LTE MIMO 2x2 3G Rx diversity</td>
<td>No RF functional difference Different operating bands support</td>
</tr>
<tr>
<td>88-90</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>91</td>
<td>RSVD</td>
<td>Reserved</td>
<td>RSVD</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>92-152</td>
<td>GND</td>
<td>Ground</td>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
</tbody>
</table>

**Table 54: TOBY-L1 and TOBY-L2 pin assignment with remarks for migration**

* Not supported by “00”, “01”, “60”, TOBY-L201-02S product versions
** Not supported by current product version
†† Not supported by “00”, “01”, “60” product versions
††† Not supported by all product versions
A.3 Schematic for TOBY-L1 and TOBY-L2 integration

Figure 85 shows an example schematic diagram where a TOBY-L1 series module or a TOBY-L2 series module ("00", "01", "02", "03", "60" or "62" product versions) can be integrated into the same application board, using all the available interfaces and functions of the module. The different mounting options for the external parts are highlighted in different colors as described in the legend, according to the interfaces supported by the different module product versions.

Figure 85: Example of complete schematic diagram to integrate TOBY-L1 modules and TOBY-L2 modules ("00", "01", "02", "03", "60", or "62" product versions) on the same application board, using all the available interfaces / functions of the modules.
## Glossary

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>3GPP</td>
<td>3rd Generation Partnership Project</td>
</tr>
<tr>
<td>8-PSK</td>
<td>8 Phase-Shift Keying modulation</td>
</tr>
<tr>
<td>16QAM</td>
<td>16-state Quadrature Amplitude Modulation</td>
</tr>
<tr>
<td>64QAM</td>
<td>64-state Quadrature Amplitude Modulation</td>
</tr>
<tr>
<td>ACM</td>
<td>Abstract Control Model</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>AP</td>
<td>Application Processor</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application-Specific Integrated Circuit</td>
</tr>
<tr>
<td>AT</td>
<td>AT Command Interpreter Software Subsystem, or attention</td>
</tr>
<tr>
<td>BAW</td>
<td>Bulk Acoustic Wave</td>
</tr>
<tr>
<td>CSFB</td>
<td>Circuit Switched Fall-Back</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DCE</td>
<td>Data Communication Equipment</td>
</tr>
<tr>
<td>DDC</td>
<td>Display Data Channel interface</td>
</tr>
<tr>
<td>DL</td>
<td>Down-Link (Reception)</td>
</tr>
<tr>
<td>DRX</td>
<td>Discontinuous Reception</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processing</td>
</tr>
<tr>
<td>DTE</td>
<td>Data Terminal Equipment</td>
</tr>
<tr>
<td>ECM</td>
<td>Ethernet networking Control Model</td>
</tr>
<tr>
<td>EDGE</td>
<td>Enhanced Data rates for GSM Evolution</td>
</tr>
<tr>
<td>EMC</td>
<td>Electro-Magnetic Compatibility</td>
</tr>
<tr>
<td>EMI</td>
<td>Electro-Magnetic Interference</td>
</tr>
<tr>
<td>ESD</td>
<td>Electro-Static Discharge</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
</tr>
<tr>
<td>E-UTRA</td>
<td>Evolved Universal Terrestrial Radio Access</td>
</tr>
<tr>
<td>FDD</td>
<td>Frequency Division Duplex</td>
</tr>
<tr>
<td>FEM</td>
<td>Front End Module</td>
</tr>
<tr>
<td>FOAT</td>
<td>Firmware Over AT commands</td>
</tr>
<tr>
<td>FOTA</td>
<td>Firmware Over The Air</td>
</tr>
<tr>
<td>FTP</td>
<td>File Transfer Protocol</td>
</tr>
<tr>
<td>FW</td>
<td>Firmware</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>GNSS</td>
<td>Global Navigation Satellite System</td>
</tr>
<tr>
<td>GPIO</td>
<td>General Purpose Input Output</td>
</tr>
<tr>
<td>GPRS</td>
<td>General Packet Radio Service</td>
</tr>
<tr>
<td>GPS</td>
<td>Global Positioning System</td>
</tr>
<tr>
<td>HBM</td>
<td>Human Body Model</td>
</tr>
<tr>
<td>HSIC</td>
<td>High Speed Inter Chip</td>
</tr>
<tr>
<td>HSDPA</td>
<td>High Speed Downlink Packet Access</td>
</tr>
<tr>
<td>HSUPA</td>
<td>High Speed Uplink Packet Access</td>
</tr>
<tr>
<td>HTTP</td>
<td>HyperText Transfer Protocol</td>
</tr>
<tr>
<td>HW</td>
<td>Hardware</td>
</tr>
<tr>
<td>I/Q</td>
<td>In phase and Quadrature</td>
</tr>
<tr>
<td>I²C</td>
<td>Inter-Integrated Circuit interface</td>
</tr>
<tr>
<td>I²S</td>
<td>Inter IC Sound interface</td>
</tr>
<tr>
<td>IP</td>
<td>Internet Protocol</td>
</tr>
<tr>
<td>LDO</td>
<td>Low-Dropout</td>
</tr>
<tr>
<td>LGA</td>
<td>Land Grid Array</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
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</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>LPDDR</td>
<td>Low Power Double Data Rate synchronous dynamic RAM memory</td>
</tr>
<tr>
<td>LTE</td>
<td>Long Term Evolution</td>
</tr>
<tr>
<td>M2M</td>
<td>Machine-to-Machine</td>
</tr>
<tr>
<td>MBIM</td>
<td>Mobile Broadband Interface Model</td>
</tr>
<tr>
<td>MIMO</td>
<td>Multi-Input Multi-Output</td>
</tr>
<tr>
<td>N/A</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>N.A.</td>
<td>Not Available</td>
</tr>
<tr>
<td>NCM</td>
<td>Network Control Model</td>
</tr>
<tr>
<td>OEM</td>
<td>Original Equipment Manufacturer device: an application device integrating a u-blox cellular module</td>
</tr>
<tr>
<td>OTA</td>
<td>Over The Air</td>
</tr>
<tr>
<td>PA</td>
<td>Power Amplifier</td>
</tr>
<tr>
<td>PCM</td>
<td>Pulse Code Modulation</td>
</tr>
<tr>
<td>PCN / IN</td>
<td>Product Change Notification / Information Note</td>
</tr>
<tr>
<td>PCS</td>
<td>Personal Communications Service</td>
</tr>
<tr>
<td>PFM</td>
<td>Pulse Frequency Modulation</td>
</tr>
<tr>
<td>PMU</td>
<td>Power Management Unit</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>QPSK</td>
<td>Quadrature Phase Shift Keying</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RMII</td>
<td>Reduced Media Independent Interface</td>
</tr>
<tr>
<td>RNDIS</td>
<td>Remote Network Driver Interface Specification</td>
</tr>
<tr>
<td>RSE</td>
<td>Radiated Spurious Emission</td>
</tr>
<tr>
<td>RTC</td>
<td>Real Time Clock</td>
</tr>
<tr>
<td>SAW</td>
<td>Surface Acoustic Wave</td>
</tr>
<tr>
<td>SDIO</td>
<td>Secure Digital Input Output</td>
</tr>
<tr>
<td>SIM</td>
<td>Subscriber Identification Module</td>
</tr>
<tr>
<td>SMS</td>
<td>Short Message Service</td>
</tr>
<tr>
<td>SRF</td>
<td>Self Resonant Frequency</td>
</tr>
<tr>
<td>SSL</td>
<td>Secure Socket Layer</td>
</tr>
<tr>
<td>TBD</td>
<td>To Be Defined</td>
</tr>
<tr>
<td>TCP</td>
<td>Transmission Control Protocol</td>
</tr>
<tr>
<td>TDD</td>
<td>Time Division Duplex</td>
</tr>
<tr>
<td>TDMA</td>
<td>Time Division Multiple Access</td>
</tr>
<tr>
<td>TIS</td>
<td>Total Isotropic Sensitivity</td>
</tr>
<tr>
<td>TP</td>
<td>Test-Point</td>
</tr>
<tr>
<td>TRP</td>
<td>Total Radiated Power</td>
</tr>
<tr>
<td>UART</td>
<td>Universal Asynchronous Receiver-Transmitter</td>
</tr>
<tr>
<td>UDP</td>
<td>User Datagram Protocol</td>
</tr>
<tr>
<td>UICC</td>
<td>Universal Integrated Circuit Card</td>
</tr>
<tr>
<td>UL</td>
<td>Up-Link (Transmission)</td>
</tr>
<tr>
<td>UMTS</td>
<td>Universal Mobile Telecommunications System</td>
</tr>
<tr>
<td>USB</td>
<td>Universal Serial Bus</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>VoLTE</td>
<td>Voice over LTE</td>
</tr>
<tr>
<td>VSWR</td>
<td>Voltage Standing Wave Ratio</td>
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<tr>
<td>Wi-Fi</td>
<td>Wireless Local Area Network (IEEE 802.11 short range radio technology)</td>
</tr>
<tr>
<td>WLAN</td>
<td>Wireless Local Area Network (IEEE 802.11 short range radio technology)</td>
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<tr>
<td>WWAN</td>
<td>Wireless Wide Area Network (GSM / UMTS / LTE cellular radio technology)</td>
</tr>
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</table>
Related documents

[1] u-blox TOBY-L2 series Data Sheet, Docu No UBX-13004573
[2] u-blox MPCI-L2 series Data Sheet, Docu No UBX-13004749
[6] u-blox Firmware Update Application Note, Docu No UBX-13001845
[9] 3GPP TS 27.007 - AT command set for User Equipment (UE)
[10] 3GPP TS 27.005 - Use of Data Terminal Equipment - Data Circuit terminating; Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[12] u-blox Mux Implementation Application Note, Docu No UBX-13001887
[14] u-blox GNSS Implementation Application Note, Docu No UBX-13001849
[15] u-blox Wi-Fi / Cellular Integration Application Note, Docu No UBX-14003264
[16] PCI Express Mini Card Electromechanical Specification, Revision 2.0, April 21, 2012
[19] ETSI EN 301 489-1 - Electromagnetic compatibility and Radio spectrum Matters (ERM); EMC standard for radio equipment and services; Part 1: Common technical requirements
[20] ETSI EN 301 489-52 - Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 52: Specific conditions for Cellular Communication Mobile and portable (UE) radio and ancillary equipment
[22] 3GPP TS 34.121-2 - Technical Specification Group Radio Access Network; User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 2: Implementation Conformance Statement (ICS)
[26] u-blox End user test Application Note, Docu No UBX-13001922
[27] u-blox Package Information Guide, Docu No UBX-14001652
[28] u-blox Nested Design Application Note, Docu No UBX-16007243

Some of the above documents can be downloaded from u-blox web-site (http://www.u-blox.com/).
<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Name</th>
<th>Comments</th>
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<tr>
<td>R01</td>
<td>20-Dec-2013</td>
<td>sses</td>
<td>Initial release for TOBY-L2 series</td>
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<tr>
<td>R02</td>
<td>21-Mar-2014</td>
<td>sses</td>
<td>Initial release including MPCI-L2 series, UART and GPIOs remarked as not supported by TOBY-L2x-00S</td>
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<tr>
<td>R03</td>
<td>23-Jul-2014</td>
<td>sses</td>
<td>Updated MPCI-L2 descriptions; USB description and design-in, including VUSB_DET pin previously RSVD; MPCI-L2 thickness and installation guidelines; MPCI-L2 power-off procedure; MPCI-L2 pins 3, 5, 44, 46 definition: Not Connected instead of GPIO/GPIO; GPIOs definition and description. Additional design-in examples, minor corrections and improvements.</td>
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<tr>
<td>R04</td>
<td>30-Sep-2014</td>
<td>lpah</td>
<td>Updated FW version for Engineering Samples, Additional design-in and minor corrections</td>
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<td>R05</td>
<td>28-Nov-2014</td>
<td>lpah / sses</td>
<td>Changed status to Early Production Information</td>
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<tr>
<td>R06</td>
<td>28-Jan-2015</td>
<td>sses</td>
<td>Added description and design-in for TOBY-L2x-50S, i.e. the &quot;50&quot; product version: Updated UART, SDIO, GPIO sections</td>
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<tr>
<td>R07</td>
<td>29-May-2015</td>
<td>sses</td>
<td>Added description and design-in for TOBY-L280-00S and TOBY-L201-01S: Updated UART, FTP, HTTP, FOTA sections and any other applicable section</td>
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<tr>
<td>R09</td>
<td>19-Aug-2015</td>
<td>sses</td>
<td>Changed status to Early Production Information</td>
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<td>R10</td>
<td>30-Sep-2015</td>
<td>sses</td>
<td>Document status reverted to Advance Information</td>
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<tr>
<td>R12</td>
<td>26-Nov-2015</td>
<td>lpah</td>
<td>Document status updated to Early Production Information</td>
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<tr>
<td>R13</td>
<td>22-Dec-2015</td>
<td>sses</td>
<td>Added description and design-in for MPCI-L201-01S product versions</td>
</tr>
<tr>
<td>R14</td>
<td>31-Mar-2016</td>
<td>sses</td>
<td>Document status reverted to Advance Information</td>
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<tr>
<td>R15</td>
<td>27-Apr-2016</td>
<td>lpah</td>
<td>Document status updated to Production Information</td>
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<tr>
<td>R17</td>
<td>27-Sep-2016</td>
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<td>Document status updated to Advance Information</td>
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<tr>
<td>R18</td>
<td>21-Oct-2016</td>
<td>lpah</td>
<td>Document status updated to Early Production Information</td>
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<td>R19</td>
<td>25-Nov-2016</td>
<td>lpah</td>
<td>Extended document applicability to TOBY-L200-00S-01 / MPCI-L200-00S-01</td>
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<tr>
<td>R20</td>
<td>21-Dec-2016</td>
<td>lpah / sses</td>
<td>&quot;Disclosure restriction&quot; replaces &quot;Document status&quot; on page 2 and document footer</td>
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<td>R22</td>
<td>05-Jun-2017</td>
<td>lpah / sses</td>
<td>Updated TOBY-L201-02S product status to initial production status</td>
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<tr>
<td>R23</td>
<td>26-Jun-2017</td>
<td>lpah / sses</td>
<td>Extended document applicability to TOBY-L2, MPCI-L2 &quot;03&quot; product version</td>
</tr>
<tr>
<td>R24</td>
<td>27-Jul-2017</td>
<td>lpah</td>
<td>Updated TOBY-L200-00S-01, MPCI-L200-00S-01, TOBY-L210-00S-00, MPCI-L210-00S-00, TOBY-L210-60S-01 product status to End Of Life.</td>
</tr>
</tbody>
</table>
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